

## 10Gb/s X2 Optical Transceiver Module

### SDX4101LR-C1-M

(10GBASE-LR, 1310nm DFB, PIN-PD)

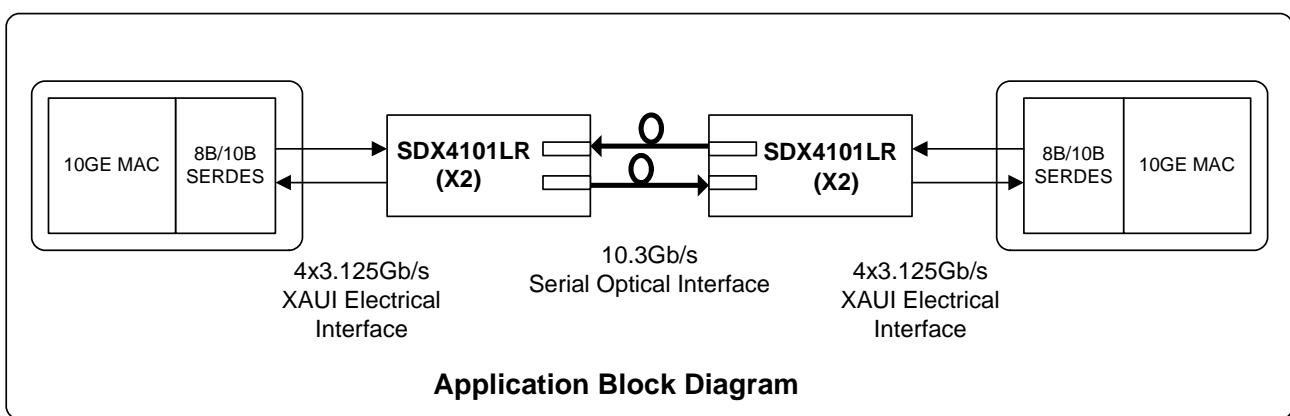
#### Features

- ◆ 10Gb/s Serial Optical Interface
  - In-house high quality and reliability optical sub-assemblies
  - 1310nm DFB laser for up to 10km over single mode fiber
  - High sensitivity PIN photo diode and TIA
- ◆ IEEE802.3ae Compliant
  - 10GBASE-LR PMD
  - XAUJ1 Electrical Interface
  - MDIO Interface for module management
- ◆ X2 MSA Issue 1.0b Compliant
  - Easy supply management for hot pluggability
  - Duplex SC Receptacle
  - Mid Personality
- ◆ XENPAK Diagnostics
  - Link Alarm Status Interrupt (LASI)
  - Diagnostic Optical Monitoring (DOM)
- ◆ Low Power Consumption
  - 1.8V and 3.3V power supply
  - Power consumption less than 4W (3.2W Typ.)



#### Applications

- ◆ 10GE Enterprise switches and routers
- ◆ 10GE Core-routers
- ◆ 10GE Storage
- ◆ Inter Rack Connection
- ◆ Other high speed data connections





## 1. General Description

The SDX4101LR is a very compact 10Gb/s optical transceiver module for serial 10Gigabit Ethernet applications. The SDX4101LR converts a 4x3.125Gb/s parallel electrical data streams to 10Gb/s optical output signal and a 10Gb/s optical input signal to 4x3.125Gb/s parallel electrical data streams. The 4x3.125Gb/s parallel electrical interface is fully compliant with 802.3ae XAUI specification and allows FR4 host PCB trace up to 50cm.

The SDX4101LR is designed for use in 10Gigabit Ethernet LAN (10.3Gbps) applications. The high performance uncooled 1310nm DFB-LD transmitter and high sensitivity PIN receiver provide superior performance for 10Gbit Ethernet applications up to 10km links.

The fully X2 compliant form factor provides hot pluggability, easy optical port upgrades and low EMI emission.

## 2. Functional Description

The SDX4101LR X2 transceiver is a bi-directional module with a transmitter and receiver in one package. The SDX4101LR contains a duplex SC connector for the optical interface and a 70-pin connector for the electrical interface. Figure 2.1 shows the functional block diagram of SDX4101LR X2 Transceiver

### Transmitter Operation

The transceiver module receives 4x3.125Gb/s XAUI 8B/10B encoded electrical inputs. Four lane XUAI signals are de-skewed (lane alignment) and 8B/10B decoded at PHY XS section, and reformatted into 10.3125Gb/s serial data stream by using 64B/66B encoding at the PCS and the PMA section. The Electrical to Optical (E/O) section converts an serial electrical signal to an optical signal. The optical output power is held constant by an Automatic Power Control (APC) circuit. The transmitter output can be turned off by TX\_ON/OFF signal. When TX\_ON/OFF is asserted High, Transmitter is turned on. Laser bias current and laser output power are monitored by the Diagnostic Optical Monitoring (DOM) section. The monitored values are reported through the Management Data I/O (MDIO) section with the corresponding alarm and warning status.

### Receiver Operation

The Optical to Electrical (O/E) section converts a 10.3125Gb/s optical signal to an electrical signal. The received 10.3125Gb/s 64B/66B encoded signal is converted to four 3.125Gb/s 8B/10B encoded XAUI electrical signals after 64B/66B decoding at the PCS section.

Receive optical power is monitored by the DOM section. The monitored value is reported through the MDIO section with the corresponding alarm and warning status.

### Management Data I/O (MDIO)

The SDX4101LR support the MDIO interface specified in IEEE802.3ae Clause 45. This 2-wire Management Data I/O interface is provided for the module status monitoring and

## Preliminary Specification

control. The Management Data Clock (MDC) provides clocking for the data that is passed on the MDIO port. Five further pins allow for loading of a port address (PRTAD0-4) into the module.

In addition to the register needed to support IEEE802.3ae standard, SDX4101LR provides some information specific to X2 module in a set of Non-Volatile Resistors (NVR). That information can be read via the MDC/MDIO port. Example of information contained in the NVR includes the identification of the module such as manufacturer ID, capabilities, and version number. This information is protected from writes by the system and is intended to be programmed at manufacturer. There is also an area of NVR in the SDX4101LR that can be read and written by the system.

### Link Alarm Status Interrupt (LASI)

The Link Alarm Status Interrupt (LASI) is an active “Low” output that indicates a link fault condition has been asserted. SDX4101LR has the status registers for fault occurrences on the transmitter, receiver and link status, support the MDIO interface specified in IEEE802.3ae Clause 45. This 2-wire Management Data I/O interface is provided for the module status monitoring and control. MDC provides clocking for the data that is passed on the MDIO port. Five further pins allow for loading of a port address (PRTAD0-4) into the module.

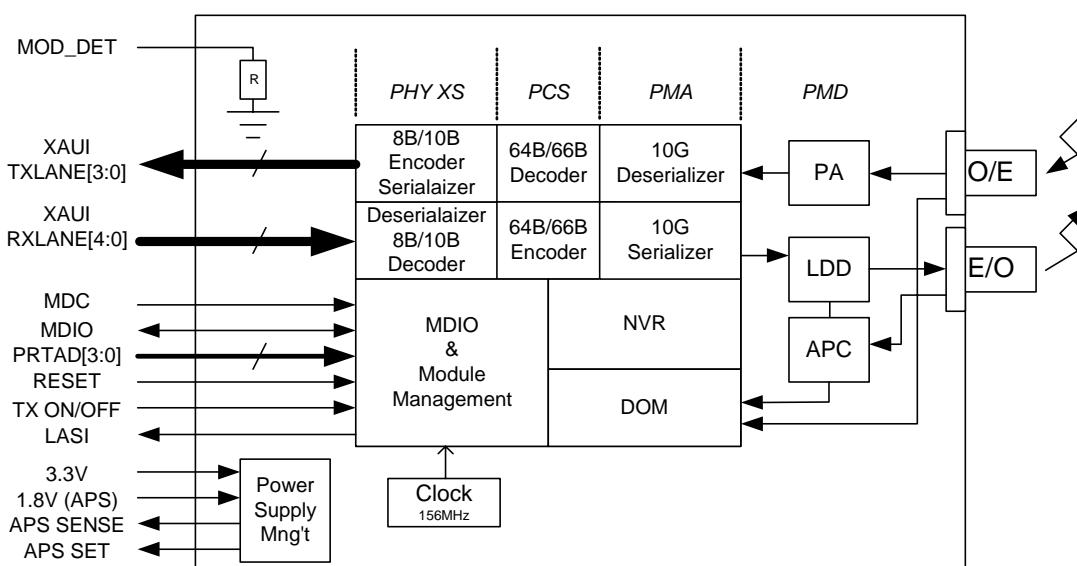


Figure 2.1 Functional Block Diagram

### 3. Package Dimensions

Figure 3.1 shows the package dimensions of SDX4101LR. The SDX4101LR transceiver is designed to be complaint with X2 MSA specification. Package dimensions are specified in section 6 of the X2 MSA specification Rev.1.0b.

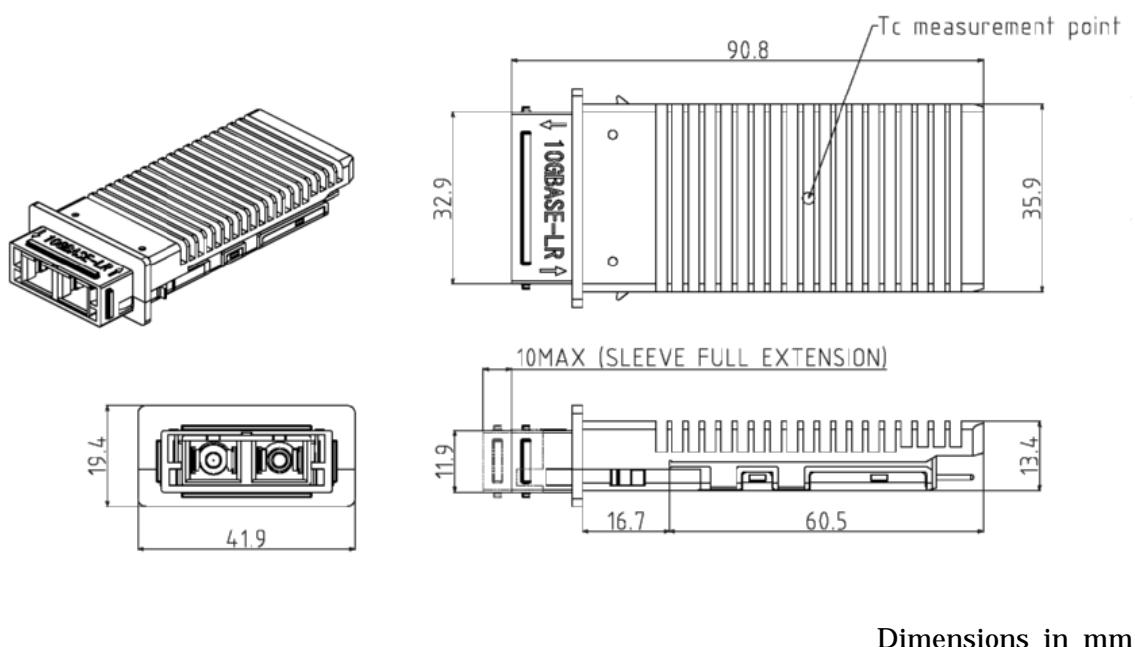


Figure 3.1 Package dimensions –Middle Personality–

## 4. Pin Assignment and Pin Description

### 4.1. X2 Transceiver Electrical Pad Layout

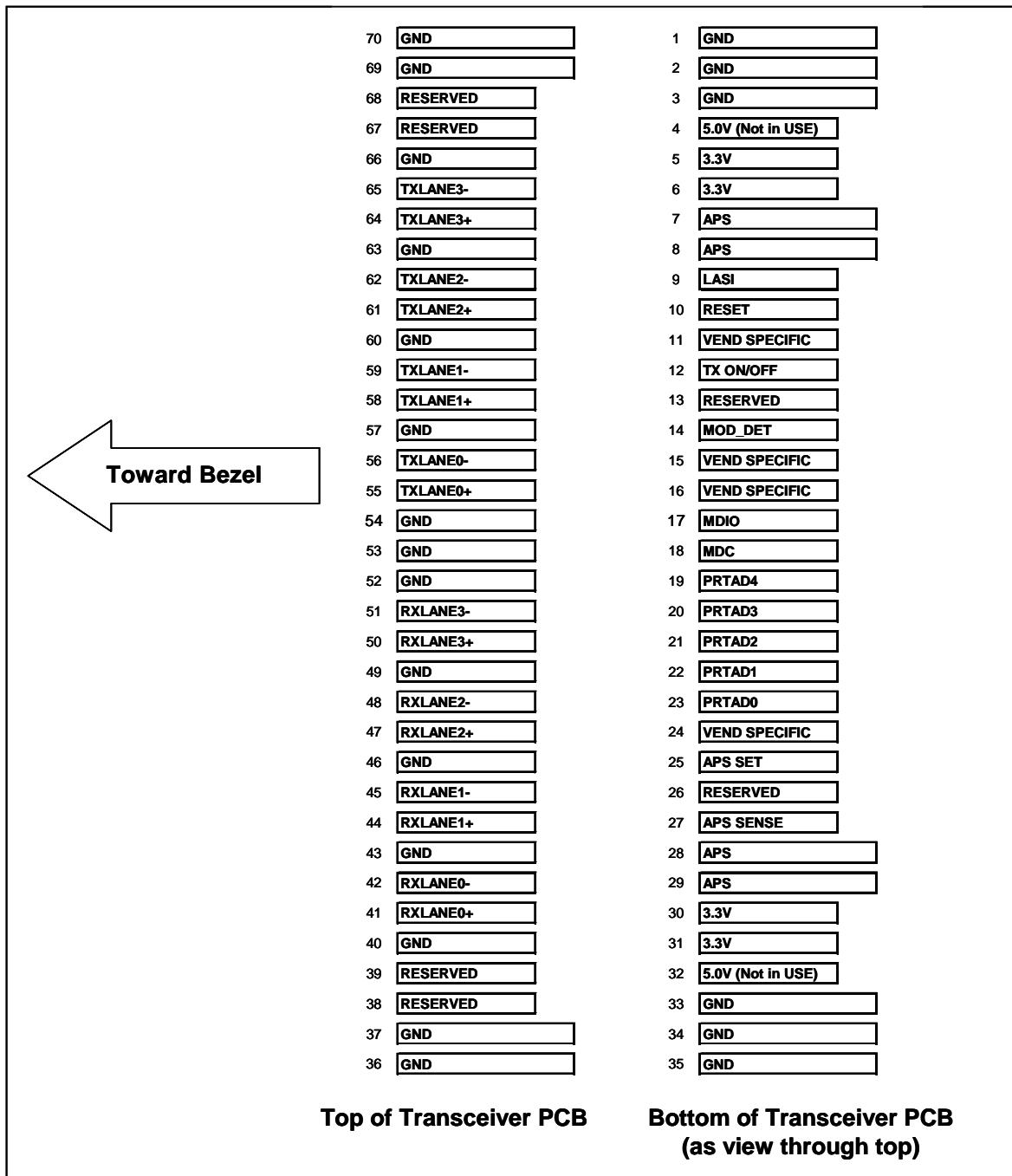


Figure 4.1 X2 Transceiver Electrical Pad Layout

#### **4.2. Host PCB X2 Pinout**

1	GND	GND	70
2	GND	GND	69
3	GND	RESERVED	68
4	5.0V (Not in USE)	RESERVED	67
5	3.3V	GND	66
6	3.3V	TXLANE3-	65
7	APS	TXLANE3+	64
8	APS	GND	63
9	LASI	TXLANE2-	62
10	RESET	TXLANE2+	61
11	VEND SPECIFIC	GND	60
12	TX ON/OFF	TXLANE1-	59
13	RESERVED	TXLANE1+	58
14	MOD_DET	GND	57
15	VEND SPECIFIC	TXLANE0-	56
16	VEND SPECIFIC	TXLANE0+	55
17	MDIO	GND	54
18	MDC	GND	53
19	PRTAD4	GND	52
20	PRTAD3	RXLANE3-	51
21	PRTAD2	RXLANE3+	50
22	PRTAD1	GND	49
23	PRTAD0	RXLANE2-	48
24	VEND SPECIFIC	RXLANE2+	47
25	APS SET	GND	46
26	RESERVED	RXLANE1-	45
27	APS SENSE	RXLANE1+	44
28	APS	GND	43
29	APS	RXLANE0-	42
30	3.3V	RXLANE0+	41
31	3.3V	GND	40
32	5.0V (Not in USE)	RESERVED	39
33	GND	RESERVED	38
34	GND	GND	37
35	GND	GND	36

**Figure 4.2 Host PCB X2 Pinout**



#### 4.3. Pin Descriptions

**Table 4.3.1 Pin Description**

Pin#	Name	I/O	Pin Type	Description	Note
1	GND	-		Electrical Ground	1
2	GND	-		Electrical Ground	1
3	GND	-		Electrical Ground	1
4	5.0V	-		Not in use. Not connected internally	
5	3.3V	-		POWER +3.3V	
6	3.3V	-		POWER +3.3V	
7	APS	-		APS POWER (+1.8V)	
8	APS	-		APS POWER (+1.8V)	
9	LASI	O	CMOS 1.2V Open Drain	10-22kohm pull-up on host. "H":Normal operation. , "L" : LASI asserted	
10	RESET	I	CMOS 1.2V	10-22kohm pull-up on transceiver. "H":Normal operation. , "L" : Reset	
11	VEND SPECIFIC	-		Leave unconnected. Used for manufacturing purpose	2
12	TX ON/OFF	I	CMOS 1.2V	10-22kohm pull-up on transceiver. "H":Transmitter Enable , "L" : Transmitter Off (always)	
13	RESERVED	-		Reserved	
14	MOD_DET	O		1kOhm pull-down to GND on transceiver	
15	VEND SPECIFIC	-		Leave unconnected. Used for manufacturing purpose	2
16	VEND SPECIFIC	-		Leave unconnected. Used for manufacturing purpose	2
17	MDIO	I/O	CMOS 1.2V Open Drain	Management Data IO. 22kohm pull-up on host.	10-
18	MDC	I	CMOS 1.2V	Clock for Management Data IO	
19	PRTAD4	I	CMOS 1.2V	Port Address Bit 4 (Low=0)	
20	PRTAD3	I	CMOS 1.2V	Port Address Bit 3 (Low=0)	
21	PRTAD2	I	CMOS 1.2V	Port Address Bit 2 (Low=0)	
22	PRTAD1	I	CMOS 1.2V	Port Address Bit 1 (Low=0)	
23	PRTAD0	I	CMOS 1.2V	Port Address Bit 0 (Low=0)	
24	VEND SPECIFIC	-		Leave unconnected. Used for manufacturing purpose	2
25	APS SET	I		Feedback input for APS	
26	Reserved	-		Reserved for APD use	
27	APS SENSE	I		APS Sense Connection	
28	APS	-		APS POWER (+1.8V)	
29	APS	-		APS POWER (+1.8V)	
30	3.3V	-		POWER +3.3V	
31	3.3V	-		POWER +3.3V	
32	5.0V	-		Not in use. Not connected internally	
33	GND	-		Electrical Ground	1
34	GND	-		Electrical Ground	1
35	GND	-		Electrical Ground	1



Pin#	Name	I/O	Pin Type	Description	Note
36	GND	-		Electrical Ground	1
37	GND	-		Electrical Ground	1
38	RESERVED	-		Reserved	
39	RESERVED	-		Reserved	
40	GND	-		Electrical Ground	1
41	RXLANE0+	O	XAUI	RX XAUI Output Lane0 +	
42	RXLANE0-	O	XAUI	RX XAUI Output Lane0 -	
43	GND	-		Electrical Ground	1
44	RXLANE1+	O	XAUI	RX XAUI Output Lane1 +	
45	RXLANE1-	O	XAUI	RX XAUI Output Lane1 -	
46	GND	-		Electrical Ground	1
47	RXLANE2+	O	XAUI	RX XAUI Output Lane2 +	
48	RXLANE2-	O	XAUI	RX XAUI Output Lane2 -	
49	GND	-		Electrical Ground	1
50	RXLANE3+	O	XAUI	RX XAUI Output Lane3 +	
51	RXLANE3-	O	XAUI	RX XAUI Output Lane3 -	
52	GND	-		Electrical Ground	
53	GND	-		Electrical Ground	1
54	GND	-		Electrical Ground	1
55	TXLANE0+	I	XAUI	TX XAUI Input Lane0 +	
56	TXLANE0-	I	XAUI	TX XAUI Input Lane0 -	
57	GND	-		Electrical Ground	1
58	TXLANE1+	I	XAUI	TX XAUI Input Lane1 +	
59	TXLANE1-	I	XAUI	TX XAUI Input Lane1 -	
60	GND	-		Electrical Ground	1
61	TXLANE2+	I	XAUI	TX XAUI Input Lane2 +	
62	TXLANE2-	I	XAUI	TX XAUI Input Lane2 -	
63	GND	-		Electrical Ground	1
64	TXLANE3+	I	XAUI	TX XAUI Input Lane3 +	
65	TXLANE3-	I	XAUI	TX XAUI Input Lane3 -	
66	GND	-		Electrical Ground	1
67	RESERVED	-		Reserved	
68	RESERVED	-		Reserved	
69	GND	-		Electrical Ground	1
70	GND	-		Electrical Ground	1

## Note

- 1: Module ground pins are isolated from the module case and chassis ground within the module.
- 2: Transceiver will be MSA compliant when no signals are present on the vendor specific pins.



## 5. Absolute Maximum Ratings and Recommended Operating Conditions

**Table 5.1 Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit	Note
Strage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH		85	%	
Operating Case Temperature	Topc	0	70	degC	1
Short-term operating case temperature	Top-short	-5	75	degC	2
Supply Voltage	3.3V	-0.5	3.6	V	
Supply Voltage	APS		2	V	
Voltag on any XAUI pin	V <sub>XAU</sub> I		2.5	V	
Voltage on any LVCMOS pin	V <sub>LVCMOS</sub>	-0.7	4	V	
Receiver Input Optical Power	Mip		2	dBm	3

Note:

- 1: Ta: -5 to 55degC with 1.5m/s airflow.
- 2: Performance is not guaranteed. The short term temperature range will not occur continuously, but only during a period of maximum 15 days per year of which 4 days maximum continuously.
- 3: PIN Receiver

**Table 5.2 Recommended Operating Conditions and supply requirements**

Parameter	Symbol	Min	Max	Unit	Note
Operating Case Temperature	Topc	0	70	degC	
Relative Humidity (non-condensing)	Rhop		85	%	
Power Supply Voltage	3.3V	3.135	3.465	V	
Power Supply Voltage	APS	1.728	1.872	V	
Power Supply Current for 3.3V			900	mA	
Power Supply Current for APS			2000	mA	
Total Power Consumption	Pd	-	4	W	

## 6. Electrical Interface

### 6.1 Electrical High Speed I/O Interface

**Table 6.1 XAUI Input Interface**

XAUI Receiver Parameters	symbol	Min	Typ	Max	Units	Note
BAUD Rate			3.125		Gb/s	
BAUD Rate tolerance		-100		100	ppm	
Differential Input signal Amplitude	Vinswing	100		2500	mVp-p	
Differential Input Impedance	Zd		100		Ohm	
Differential Return Loss	RLd	10			dB	1
Common mode Return Loss	RLcm	6			dB	
Jitter Amplitude Tolerance		0.55+SJ			Ulpp	2

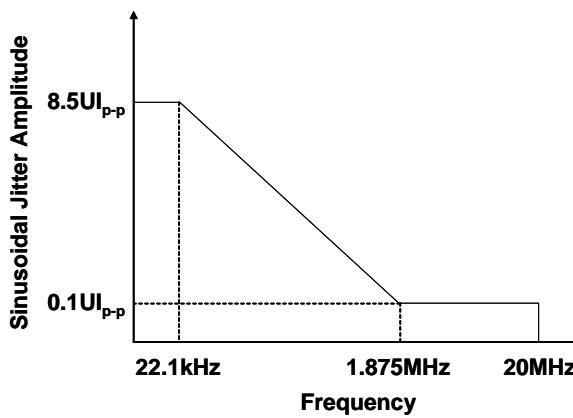
**Table 6.2 XAUI Output Interface**

XAUI Driver Parameters	symbol	Min	Typ	Max	Units	Note
BAUD Rate			3.125		Gb/s	
BAUD Rate tolerance		-100		100	ppm	
Differential Output Signal Amplitude	Voswing	800		1600	mVp-p	
Transition Times (20 - 80%)		60		130	ps	
Total Output jitter	Tjo	-0.175		0.175	UI	
Output Differential Skew	SKWd			15	ps	
Electrical Eye Mask (Near End)	A1	400			mV	3
	A2	800			mV	
	X1	0.175			UI	
	X2	0.39			UI	

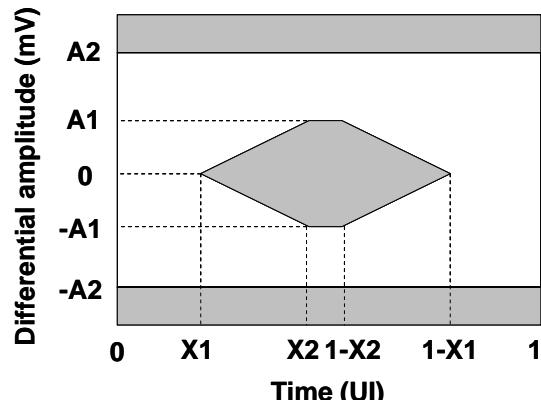
Note1: 100MHz to 2.5GHz

Note2: Refer to Fig.6.1

Note3: Refer to Fig.6.2



**Fig 6.1 Single-tone sinusoidal jitter(SJ) mask**



**Fig 6.2 Driver Template**

## 6.2 Electrical Low Speed I/O Interface

**Table 6.2.1 1.2V CMOS DC parameters**  
**(LASI, RESET, TXONOFF, MDC, PRTAD<4:0>)**

Parameter	symbol	Min	Typ	Max	Units	Note
Output High Voltage	Voh	1		1.5	V	
Output Low Voltage	Vol	-0.3		0.2	V	
Output Low Current (Vi = 0.3V)	Iol	-4			mA	
Input High Voltage	Vih	0.84		1.5	V	
Input Low Voltage	Vil	-0.3		0.36	V	

**Table 6.2.2 1.2V CMOS DC parameters (MDIO)**

Parameter	symbol	Min	Typ	Max	Units	Note
Output High Voltage	Voh	1		1.5	V	
Output Low Voltage	Vol	-0.3		0.2	V	
Output low current (Vi = 0.3V)	Iol	-4			mA	
Input High Voltage	Vih	0.84		1.5	V	
Input Low Voltage	Vil	-0.3		0.36	V	
Input Capacitance	Ci			10	pF	
Bus Loading	CL			470	pF	

**Table 6.2.3 MDIO and MDC AC parameters**

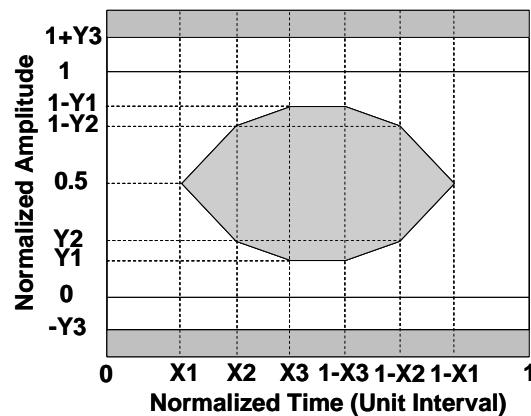
Parameter	symbol	Min	Typ	Max	Units	Note
MDIO data hold time	Thold	10			ns	
MDIO data setup time	Tsetup	10			ns	
Delay from MDC rising edge to MDIO data change	Tdelay			300	ns	
MDC clock rate	Fmax			2.5	MHz	

## 7. Optical Interface

**Table 7.1 Optical Interface**

Transmitter Optical Interface						
Parameter	Symbol	Min	Typical	Max	Unit	Note
Operating Data Rate	-		10.3125		Gb/s	
Data rate tolerance		-100		100	ppm	
Output Center Wavelength	l <sub>tc</sub>	1260		1355	nm	
SMSR	SMSR	30		-	dB	
Average Output Power	P <sub>o</sub>	-6		-1	dBm	
Extinction Ratio	ER	3.5	5	-	dB	
Optical Modulation Amplitude (OMA)	OMA	-5.2		-	dBm	
Transmitter and Dispersion Penalty (TDP)	TDP			3.2	dB	
OMA-TDP	OMAtdp	-6.2		-	dBm	
Eye Mask {X <sub>1</sub> , X <sub>2</sub> , X <sub>3</sub> , Y <sub>1</sub> , Y <sub>2</sub> , Y <sub>3</sub> }		{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}			1	
RIN <sub>12</sub> OMA	RIN			-128	dB/Hz	
Optical Return Loss Tolerance		12			dB	
Transmitter Refractance				-12	dB	
Receiver Optical Interface						
Operating Data Rate	-		10.3125		Gb/s	
Data rate tolerance		-100		100	ppm	
Input Center Wavelength	l <sub>rc</sub>	1260		1355	nm	
Sensitivity	P <sub>imin</sub>			-14.4	dBm	
Stressed Sensitivity in OMA	OMAst			-10.3	dBm	
Sensitivity in OMA	OMA0			-12.6	dBm	
Overload	R <sub>ovl</sub>	0.5		-	dBm	
Receiver Damage Power	R <sub>rdmg</sub>	1.5			dBm	
Signal Detect On	S <sub>don</sub>	-30		-	dBm	
Signal Detect Off	S <sub>doff</sub>			-16	dBm	
Signal Detect Hysteresis	S <sub>dhys</sub>	0.5			dB	
Optical Return Loss	ORL	14		-	dB	

Note1: Refer to Fig.7.1.



**Fig 7.1 Transmission eye mask definition**



## 8. Qualification Testing

The SDX4101LR Series 10Gb/s transceivers are qualified to Sumitomo Electric Industries internal design and manufacturing standards. Telecordia GR-468-CORE reliability test standards, using methods per MIL-STD-883 for mechanical integrity, endurance, moisture, flammability and ESD thresholds, are followed.

## 9. Laser Safety Information

The SDX4101LR Series transceivers use a semiconductor laser that is classified as Class 1 laser products per the Laser Safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC 60825-1 International standards.

### Caution

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If this product is used under conditions not recommended in the specification or is used with unauthorized revision, the classification for laser product safety is invalid. Reclassify the product at your responsibility and take appropriate safety measures.

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## 10. Electromagnetic Compatibility

### EMI (Emission)

The SDX4101LR Series 10Gb/s transceivers are designed to meet FCC Class B limits for emissions and noise immunity per CENELEC EN50 081 and 082 specifications.

### RF Immunity

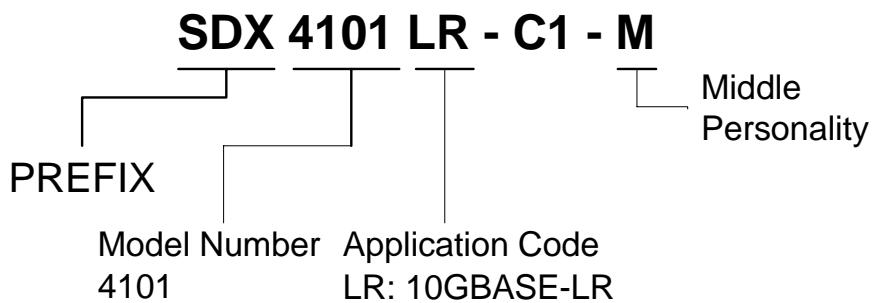
The SDX4101LR has an immunity to operate when tested in accordance with IEC 61000-4-3 (80- 1000MHz, Test Level 3) and GR-1089.

### Electrostatic Discharge (ESD) Immunity

The SDX4101LR has an immunity against direct and indirect ESD when tested accordance with IEC 61000-4-2.

## 11. Ordering Information

### 11.1. Part Numbering System



### 11.2. Evaluation Board Kit

For test purposes, Evaluation Board model number SK4101A may be ordered to use with the SDX4101LR Series transceivers.

SK4101A : SDX4101 X2 evaluation board

## 12. Ordering Number Code

**Table 13. SDX4101LR Application Code**

P/N	Distance	Fiber	E/O	O/E	ITU-T G.691	Telecordia GR-253	IEEE 802.3ae
SDX4101LR-C1-M	10km	STD-SMF	1.31mm DFB	PIN	-	-	10GBASE-LR



### 13. Contact Information

#### **U.S.A.**

ExceLight Communications, 4021 Stirrup Creek Drive, Suite 200 Durham, NC 27703  
Tel. +1-919-361-1600 / Fax. +1-919-361-1619  
E-mail: info@excelight.com  
<http://www.excelight.com>

#### **Europe**

Sumitomo Electric Europe Ltd., 220, Centennial Park, Elstree, Herts, WD6 3SL, United Kingdom  
Tel. +44-208-953-8681  
Fax. +44-208-207-5950  
E-mail: [photonics@sumielectric.com](mailto:photonics@sumielectric.com)  
<http://www.sumielectric.com>

#### **Japan**

Sumitomo Electric Industries, Ltd. (Photo-Electron Products Division)  
1, Taya-cho, Sakae-ku, Yokohama, 244-8588  
Tel. +81-45-853-7154 / Fax. +81-45-851-1932  
E-mail: [product-info@ppd.sei.co.jp](mailto:product-info@ppd.sei.co.jp)  
[http://www.sei.co.jp/Electro-optic/index\\_e.html](http://www.sei.co.jp/Electro-optic/index_e.html)