Technical Specifications (Rev 0.0 /Dec, 2008)

TRT7063ENabcSM-x,

DWDM-X2 Transceiver

All specifications described herein are subject to change due to continuous improvements.

Sample Categories and Disclaimer

Functional sample that has the suffix of "-F" or "-Fx" to the product number is a sample that is designed according to the customer's request. The purpose of this sample is to check and confirm the product feasibility. Thus the sample may be an R&D prototype or may be a modified current product. This sample may not be manufactured in qualified production lines nor using qualified parts. Basically Opnext guarantees the requested performance of BOL (Beginning Of Life). Any qualification will not be applied.

Working sample that has the suffix of "-W" or "-Wx" to the product number is a sample to evaluate, confirm and finalize the product specifications. Basically Opnext guarantees the performance of BOL (Beginning Of Life). Not all qualifications may be completed. This sample may not be manufactured in qualified production lines nor be using qualified components. Until Opnext Inc. releases the products for general sales, Opnext Inc. reserves the right to change prices, features, functions, specifications, capabilities and release schedule.

FEATURES

- **ITU-T C band 100GHz DWDM**
- **80 km Transmission Distance**
- **High performance cooled 1550 nm EA-DFB TOSA and APD ROSA**
- **XAUI Electrical Interface: 4 Lanes @ 3.125Gbit/s**
- **X2 MSA compliant**
- **MDIO, DOM Support**
- **Operating Case Temperature: 0 to 70 °C**
- **Low power consumption: < 4W (5 V, 3.3 V and APS=1.25 V)**

REFERENCE

IEEE 802.3ae as 10GBASE X2 MSA Release 2.0b

DESCRIPTION

General

The TRT7063ENabcSM is a 10GbE X2 type DWDM transceiver module which can transmit up to 80 km (1,600 ps/nm) with ITU-T on grid wavelength. It is compliant with X2 MSA for the physical and electrical interfaces and therefore has a feature of hot pluggable function in the Z-direction. It is applicable to typical router line card, Storage, IP network and LAN. For detailed MDIO default setting, please refer to the attachment.

The TRT7063ENabcSM is a fully integrated 10.3125Gbit/s optical transceiver module that consists of optical transmitter and receiver, Mux and Demux with clock and data recovery (CDR) and XAUI interface. The TRT7063ENabcSM uses 1550nm EA-DFB TOSA and APD ROSA to achieve high quality performances over 80 km standard single mode fiber.

SPECIFICATIONS

Block Diagram

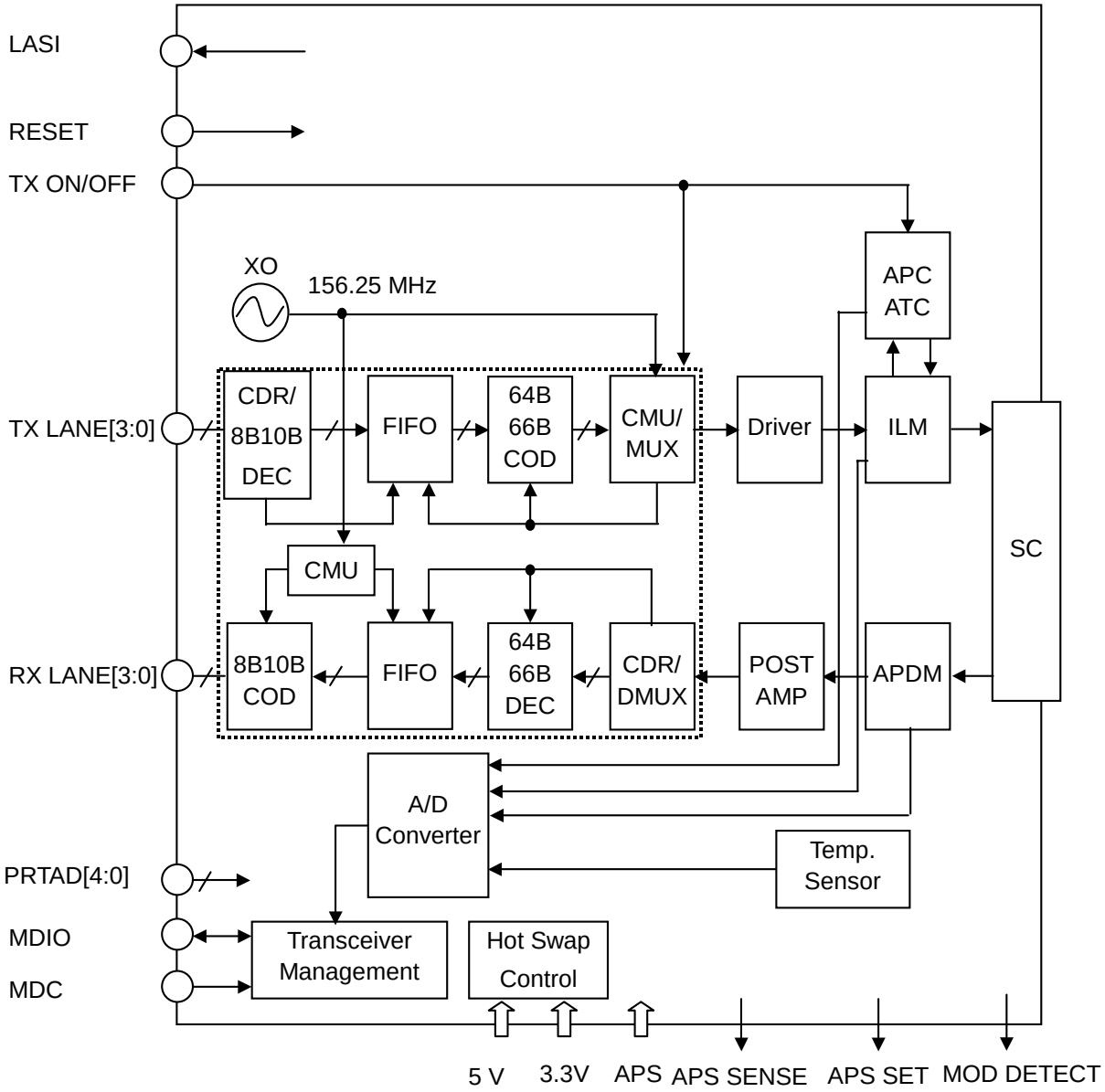

Figure 1 Schematic block diagram of the transceiver

Functional Description

(1) XAUI Data Interface

No.	Symbol	Function	I/O	Logic	Remarks
1	TX LANE[3:0]	XAUI Differential Input Data	I	XAUI	
2	RX LANE[3:0]	XAUI Differential Output Data	O	XAUI	

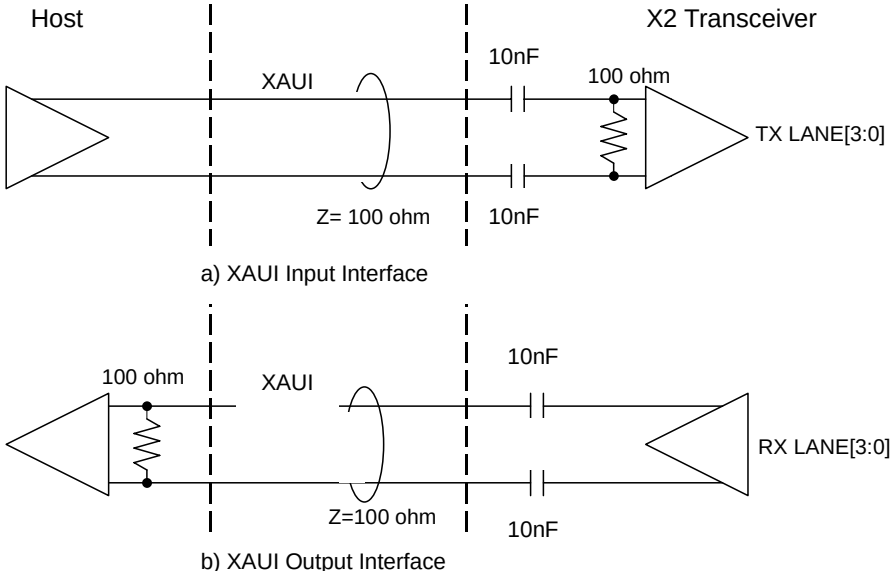

Figure 2 Interface to Host

(2) MDIO Data and Clock

No.	Symbol	Function	I/O	Logic	Remarks
1	MDIO	Management Data I/O	I/O	Open drain	Figure 5
2	MDC	Management Data Clock	I	1.2V CMOS	

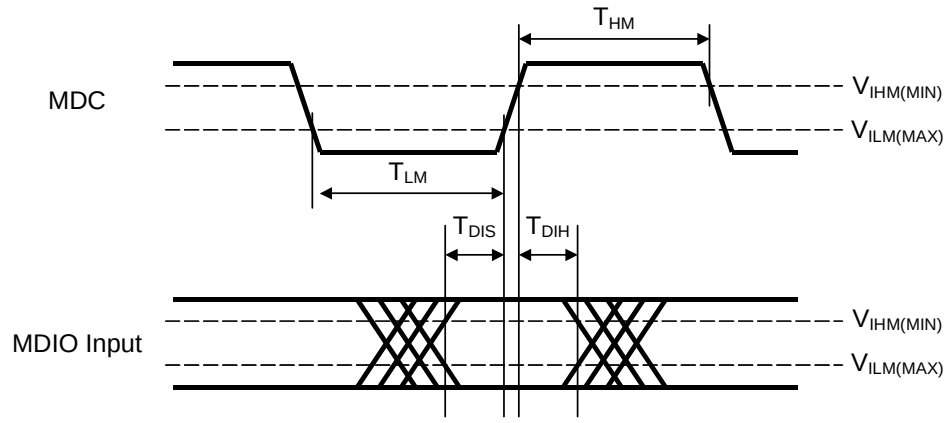

Figure 3 MDC and MDIO timing waveforms during MDIO input

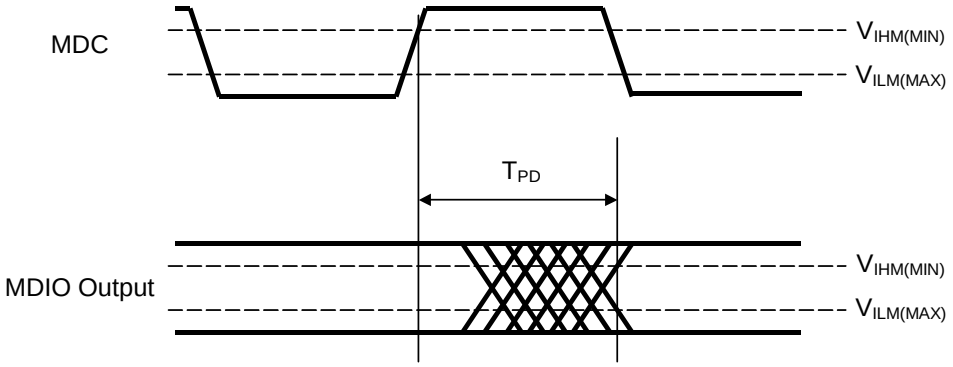

Figure 4 MDC and MDIO timing waveforms during MDIO output

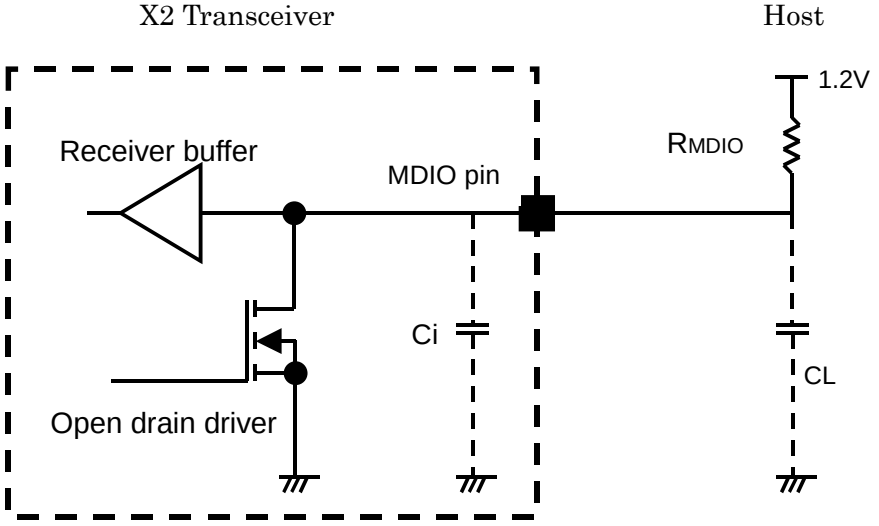

Figure 5 MDIO Interface

(3) APS/APS SENSE

No.	Symbol	Function	I/O	Logic	Remarks
1	APS	Adaptive Power Supply	I	Supply	
2	APS SENSE	APS Sense Connection	O	Analog	

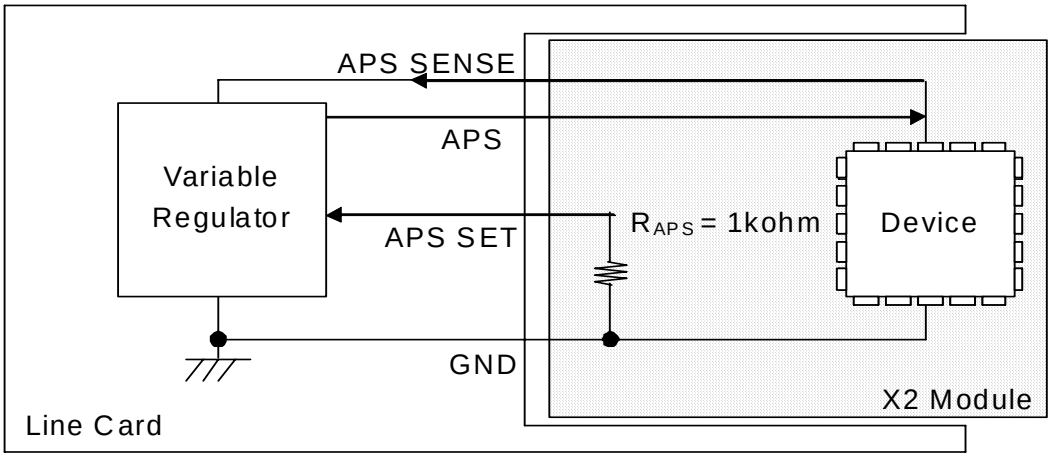

Figure 6 Adaptable Power Supply

(4) Initialization Timing after the Power ON

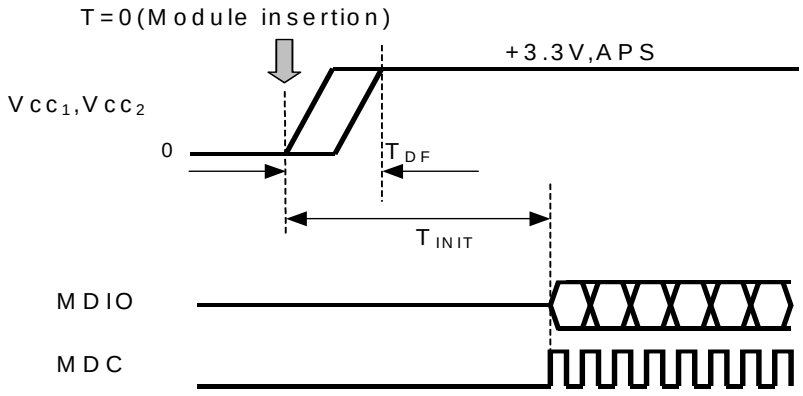

Figure 7 Initialization Timing Diagram after the Power ON

(5) LASI (Link Alarm Status Interrupt)

No.	LASI	Function	Remarks
1	H	Normal Operation	Open Drain
2	L	LASI Asserted	

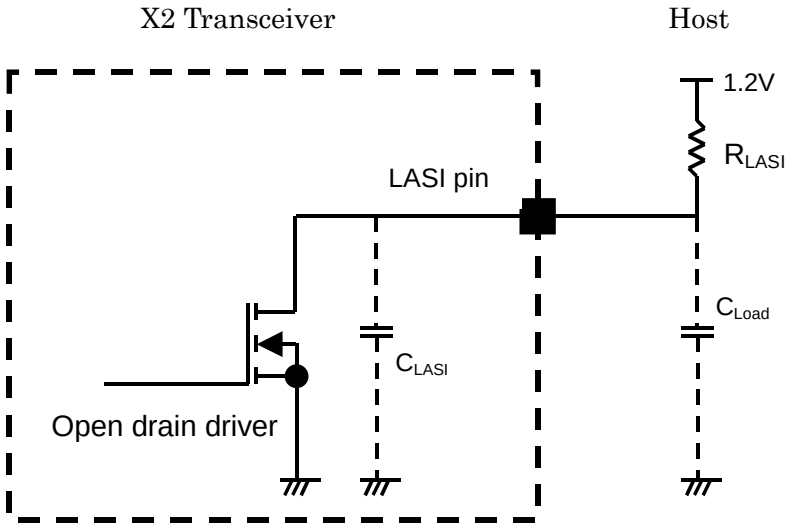

Figure 8 LASI Interface

(6) RESET

No.	RESET pin (Pin No.10) Condition	MDIO Register Condition 1.0.15(Reset bit)	Function	Remarks
1	H	0	Normal Operation	RESET pin (Pin No.10) 1.2V CMOS
2	L *	0	Reset	
3	H	1		
4	L *	1		

* Note: TX off when RESET pin, pin number 10, is “L”.

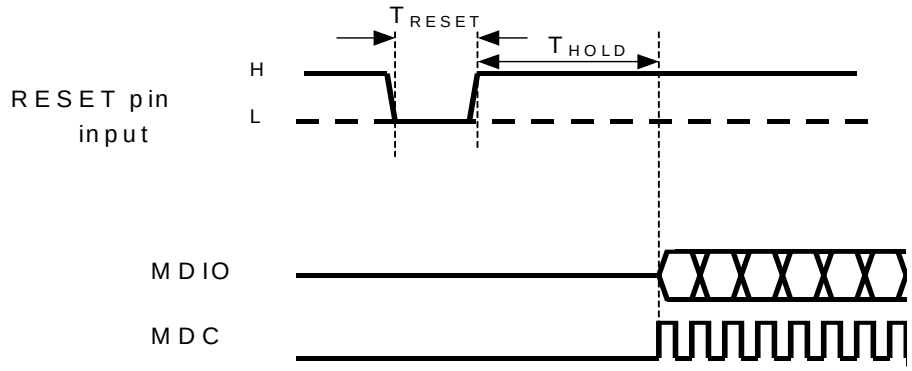

Figure 9 RESET pin and MDIO/MDC Timing Diagram

(7) TX ON/OFF(pin12)

No.	TX ON/OFF	Function	Remarks
1	H	Tx ON	1.2V CMOS.
2	L	Tx OFF	MDIO active in both TX ON/OFF status.

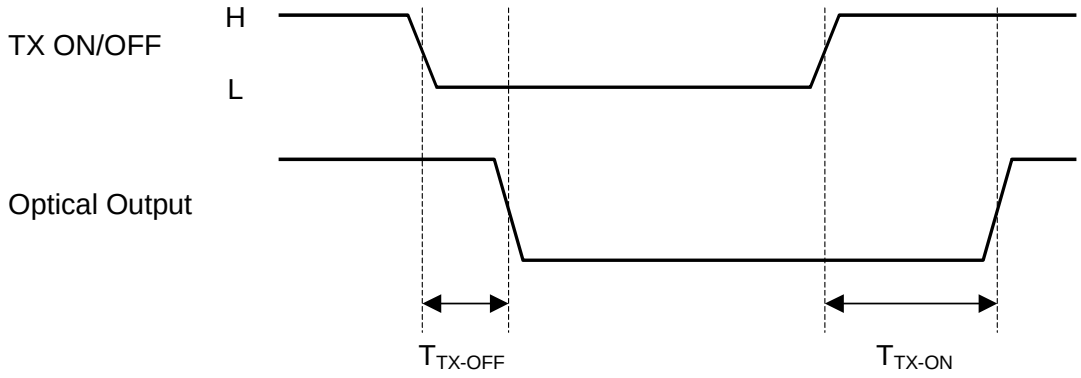

Figure 10 Tx OFF to Optical Output Timing Diagram

(8) Inrush currents on fixed power supply

No.	Parameter	Symbol	Min.	Max.	Unit	Remarks
1	Icc peak Inrush	Icc_peak	-	150	%	+3.3V
2	Icc ramp rate	ΔIcc/Δt	-	50	mA/ms	+3.3V

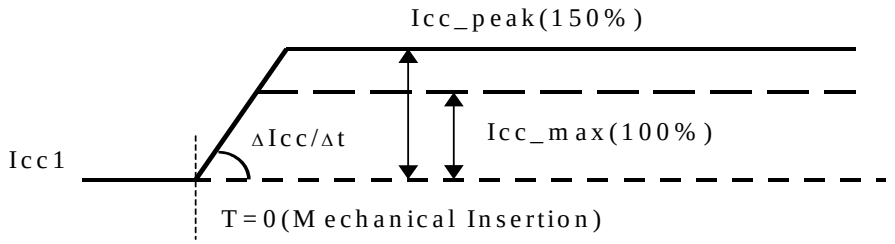

Figure 11 Inrush current transitional characteristics

PERFORMANCE SPECIFICATIONS

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the transceiver.

Table 1. Absolute Maximum Ratings

No.	Parameter	Symbol	Min.	Max.	Unit	Remarks
1	Supply Voltage	V_{CC5}	0	+6	V	+5V
2	Supply Voltage	V_{CC3}	0	+3.6	V	+3.3V
3	Supply Voltage	V_{APS}	0	+1.5	V	APS
4	Optical Receiver Input	P_{IMAX}	-	-1	dBm	
5	Case Temperature	Tc	0	+70	°C	Figure 12
6	Storage Temperature	T_{STR}	-40	+85	°C	

Operating Environment

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Table 2. Operating Environment

No.	Parameter	Symbol	Min.	Typ	Max	Unit	Remarks
1	Supply Voltage	V_{CC5}	4.75	5.000	5.25	V	+5V
2	Supply Voltage	V_{CC3}	3.135	3.300	3.465	V	+3.3V
3	Supply Voltage	V_{APS}	1.20	1.250	1.30	V	APS
4	Case Temperature	T_C	0	25	70	°C	Figure 12

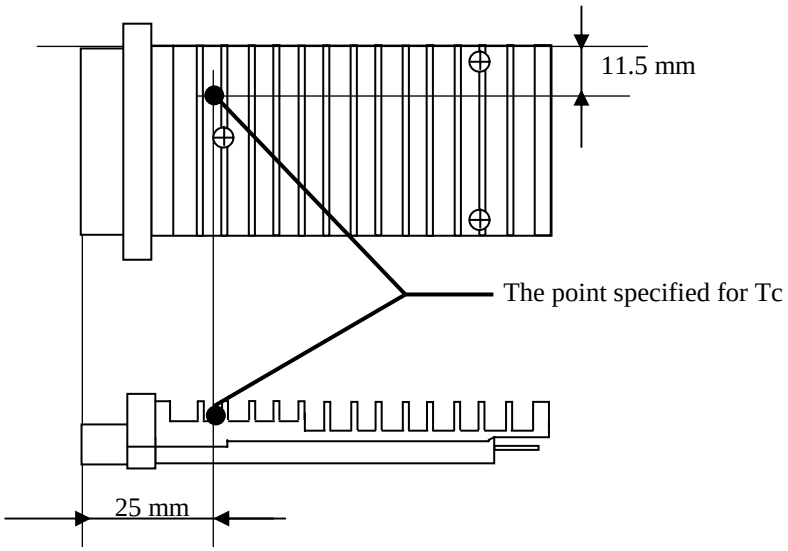

Figure 12 Tc test point

Optical Characteristics

Table 3. Optical Characteristics

No	Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
1	Center Wavelength	λ_C	1530.33	-	1560.61	nm	ITU-T grid Ch21 to ch59
2	Wavelength stability	λ_s	-	-	+/-100	pm	Selected grid
3	Signaling speed	f_{Dn}	-	10.3125	-	Gbit/s	
5	Signaling variation		-100	-	+100	ppm	
6	Optical Output Power	P_f	-1	-	+3	dBm	
7	Optical Waveform	-	Figure 13			-	
8	SMSR	S_r	30	-	-	dB	
9	Extinction Ratio	E_r	8.2	-	-	dB	
10 a	Off Transmit Power	P_{off}	-	-	-30	dBm	Average
10 b	Optical Output turn-on Time	T_{TX-ON}	-	-	100	ms	
11	Optical Output turn-off Time	T_{TX-OFF}	-	-	1	ms	Figure9
12	Receiving wavelength	λ_{Rx}	1530	-	1560	nm	
13	Receiver Overload	R_{OL}	-7	-	-	dBm	
14	Receiver Reflectance	R_{ref}	-	-	-27	dB	
15	Receiver sensitivity	R_{rmin}	-	-	-24	dBm	BER=1E-12, PRBS=31
16	Receiver sensitivity (@1600 ps/nm fiber)	R_{rmin}	-	-	-21	dBm	BER=1E-12, PRBS=31

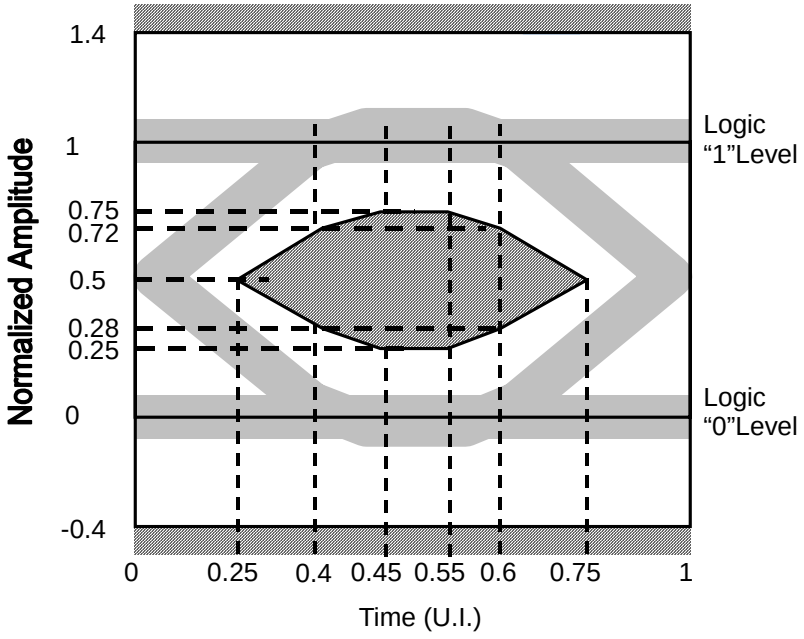

Figure 13 Mask of Eye Diagram

Electrical Performance

Table 4. Power Supply Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Supply Voltage	V_{CC5}	4.750	5.000	5.250	V	
2	Supply Voltage	V_{CC3}	3.135	3.300	3.465	V	
3	Supply Voltage	V_{APS}	1.20	1.250	1.30	V	
4	Supply Current	I_{CC5}	-	-	0.8	A	+5 V
5	Supply Current	I_{CC3}	-	-	1.4	A	+3.3 V
6	Supply Current	I_{APS}	-	-	1.7	A	APS
7	Power Consumption	P_{DS}	-	-	4.0	W	
8	Power supply stabilization time	TDF	-	-	500	ms	Figure 7
9	Initialization Time	T_{INIT}	-	-	5	s	Figure 7
10	RESET Assert Time	T_{RESET}	1	-	-	ms	Figure 9

Table 5. XAUI Driver Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Baud Rate		-	3.125	-	Gbit/s	
2	Baud Rate Tolerance		-100	-	+100	ppm	
3	Differential Amplitude		800	-	1600	mV_{PP}	AC, near-end value

Table 6. XAUI Receiver Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Baud Rate		-	3.125	-	Gbit/s	
2	Baud Rate Tolerance		-100	-	+100	ppm	
3	Differential Amplitude		200	-	1600	mVpp	AC

Table7. 1.2VCMOS Interface Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Input High Voltage	V_{IH}	0.84	-	1.5	V	
2	Input Low Voltage	V_{IL}	-0.3	-	0.36	V	
3	Input Pull-down Current	I_{In}	20	40	120	μA	Vih=1.2V
4	Output High Voltage	V_{OH}	1.0	-	-	V	Pull-up=10k ohm to 1.2V
5	Output Low Voltage	V_{OL}	-	-	0.2	V	
6	Pull up Resistance	R_{LASI}	10	-	22	k ohm	Figure 8
7	Capacitance	C_{LASI}	-	-	10	pF	Figure 8
8	Load Capacitance	C_{Load}	-	-	320	pF	Figure 8

Table8. MDIO Bidirectional Interface Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Input High Voltage	V_{IHM}	0.84	-	1.5	V	
2	Input Low Voltage	V_{ILM}	-0.3	-	0.36	V	
3	Output High Voltage	V_{OHM}	1.0	-	1.5	V	
4	Output Low Voltage	V_{OLM}	-0.3	-	0.2	V	
5	Pull up Resistance	R_{MDIO}	200	-	Note 1	Ohm	Figure 5
6	MDC min high/low time	T_{HM},T_{LM}	160	-	-	ns	Figure 3
7	MDC Frequency	$1/T_{CK}$	TBD	-	2.5	MHz	
8	Setup time	T_{DIS}	10	-	-	ns	Figure 3
9	Hold time	T_{DIH}	10	-	-	ns	Figure 3
10	MDIO output delay after rising edge of MDC	T_{PD}	0	-	300	ns	Figure 4
12	Input Capacitance	Ci	-	-	10	pF	Figure 5
13	Bus Loading	C_L	-	-	470	pF	Figure 5

Note 1 : The maximum value of R_{MDIO} depends on bus loading(C_L) , input capacitance(Ci), and MDC frequency($1/T_{CK}$).

70	GND	1	GND
69	GND	2	GND
68	RESERVED	3	GND
67	RESERVED	4	5 V
66	GND	5	3.3V
65	TX LANE3-	6	3.3V
64	TX LANE3+	7	APS
63	GND	8	APS
62	TX LANE2-	9	LASI
61	TX LANE2+	10	RESET
60	GND	11	VEND SPECIFIC
59	TX LANE1-	12	TX ON/OFF
58	TX LANE1+	13	RESERVED
57	GND	14	MOD DETECT
56	TX LANE0-	15	VEND SPECIFIC
55	TX LANE0+	16	VEND SPECIFIC
54	GND	17	MDIO
53	GND	18	MDC
52	GND	19	PRTAD4
51	RX LANE3-	20	PRTAD3
50	RX LANE3+	21	PRTAD2
49	GND	22	PRTAD1
48	RX LANE2-	23	PRTAD0
47	RX LANE2+	24	VEND SPECIFIC
46	GND	25	APS SET
45	RX LANE1-	26	RESERVED
44	RX LANE1+	27	APS SENSE
43	GND	28	APS
42	RX LANE0-	29	APS
41	RX LANE0+	30	3.3V
40	GND	31	3.3V
39	RESERVED	32	5 V

Top of Transceiver PCB Bottom of Transceiver PCB (as viewed through top)

Figure 14 X2 Pin Configuration

Table 9. Pin Description

Pin #	Symbol	I/O	Logic	Description	**Notes**
1	GND	I	Supply	Electrical ground	
2	GND	I	Supply	Electrical ground	
3	GND	I	Supply	Electrical ground	
4	5 V	I	Supply	Power	
5	3.3 V	I	Supply	Power	
6	3.3 V	I	Supply	Power	
7	APS	I	Supply	Adaptive Power Supply	1.25V
8	APS	I	Supply	Adaptive Power Supply	1.25V
9	LASI	O	Open Drain	Link Alarm Status Interrupt. 10-22k ohm pull up on host.	
10	RESET	I	1.2V CMOS	TX OFF when MDIO RESET	
11	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
12	TX ON/OFF	I	1.2V CMOS	Transmitter ON/OFF	
13	RESERVED	-	-	Reserved	
14	MOD DETECT	O	-	Pulled low inside module through 1k ohm.	
15	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
16	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
17	MDIO	I/O	Open Drain	Management Data IO	
18	MDC	I	1.2V CMOS	Management Data Clock	
19	PRTAD4	I	1.2V CMOS	Port Address bit 4 (Low=0)	
20	PRTAD3	I	1.2V CMOS	Port Address bit 3 (Low=0)	
21	PRTAD2	I	1.2V CMOS	Port Address bit 2 (Low=0)	
22	PRTAD1	I	1.2V CMOS	Port Address bit 1 (Low=0)	
23	PRTAD0	I	1.2V CMOS	Port Address bit 0 (Low=0)	
24	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
25	APS SET	O	-	Feedback output for APS	
26	RESERVED	-	-	Reserved for Avalanche Photodiode use.	
27	APS SENSE	O	Analog	APS Sense Connection	
28	APS	I	Supply	Adaptive Power Supply	
29	APS	I	Supply	Adaptive Power Supply	
30	3.3 V	I	Supply	Power	
31	3.3 V	I	Supply	Power	
32	5 V	I	Supply	Power	
33	GND	I	Supply	Electrical Ground	
34	GND	I	Supply	Electrical Ground	
35	GND	I	Supply	Electrical Ground	

Pin #	Symbol	I/O	Logic	Description	Notes
36	GND	I	Supply	Electrical Ground	
37	GND	I	Supply	Electrical Ground	
38	RESERVED	-	-	Reserved	
39	RESERVED	-	-	Reserved	
40	GND	I	Supply	Electrical Ground	
41	RX LANE 0+	O	AC	Module XAUI Output Lane 0+	
42	RX LANE 0-	O	AC	Module XAUI Output Lane 0-	
43	GND	I	Supply	Electrical Ground	
44	RX LANE 1+	O	AC	Module XAUI Output Lane 1+	
45	RX LANE 1-	O	AC	Module XAUI Output Lane 1-	
46	GND	I	Supply	Electrical Ground	
47	RX LANE 2+	O	AC	Module XAUI Output Lane 2+	
48	RX LANE 2-	O	AC	Module XAUI Output Lane 2-	
49	GND	I	Supply	Electrical Ground	
50	RX LANE 3+	O	AC	Module XAUI Output Lane 3+	
51	RX LANE 3-	O	AC	Module XAUI Output Lane 3-	
52	GND	I	Supply	Electrical Ground	
53	GND	I	Supply	Electrical Ground	
54	GND	I	Supply	Electrical Ground	
55	TX LANE 0+	I	AC	Module XAUI Input Lane 0+	
56	TX LANE 0-	I	AC	Module XAUI Input Lane 0-	
57	GND	I	Supply	Electrical Ground	
58	TX LANE 1+	I	AC	Module XAUI Input Lane 1+	
59	TX LANE 1-	I	AC	Module XAUI Input Lane 1-	
60	GND	I	Supply	Electrical Ground	
61	TX LANE 2+	I	AC	Module XAUI Input Lane 2+	
62	TX LANE 2-	I	AC	Module XAUI Input Lane 2-	
63	GND	I	Supply	Electrical Ground	
64	TX LANE 3+	I	AC	Module XAUI Input Lane 3+	
65	TX LANE 3-	I	AC	Module XAUI Input Lane 3-	
66	GND	I	Supply	Electrical Ground	
67	RESERVED	-	-	Reserved	
68	RESERVED	-	-	Reserved	
69	GND	I	Supply	Electrical Ground	
70	GND	I	Supply	Electrical Ground	

Note: Case is connected to electrical ground in the module.

Mechanical dimensions

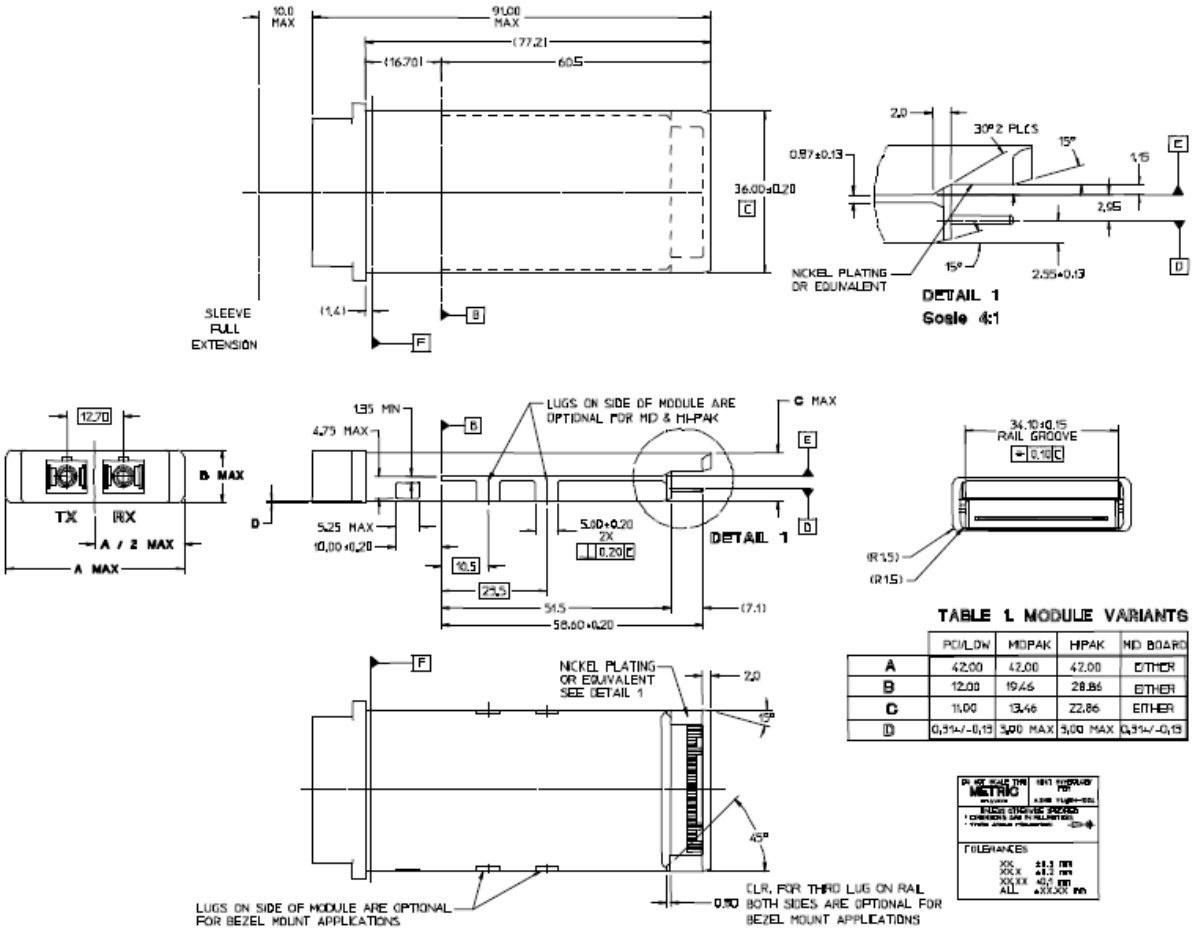

TABLE 1. MODULE VARIANTS

	PCI/LDN	MDPAK	HPAK	MD BOARD
A	42.00	42.00	42.00	EITHER
B	12.00	19.46	28.86	EITHER
C	11.00	13.46	22.86	EITHER
D	0.914+/-0.13	3.00 MAX	3.00 MAX	0.914+/-0.13

Figure 15 Mechanical dimensions on X2

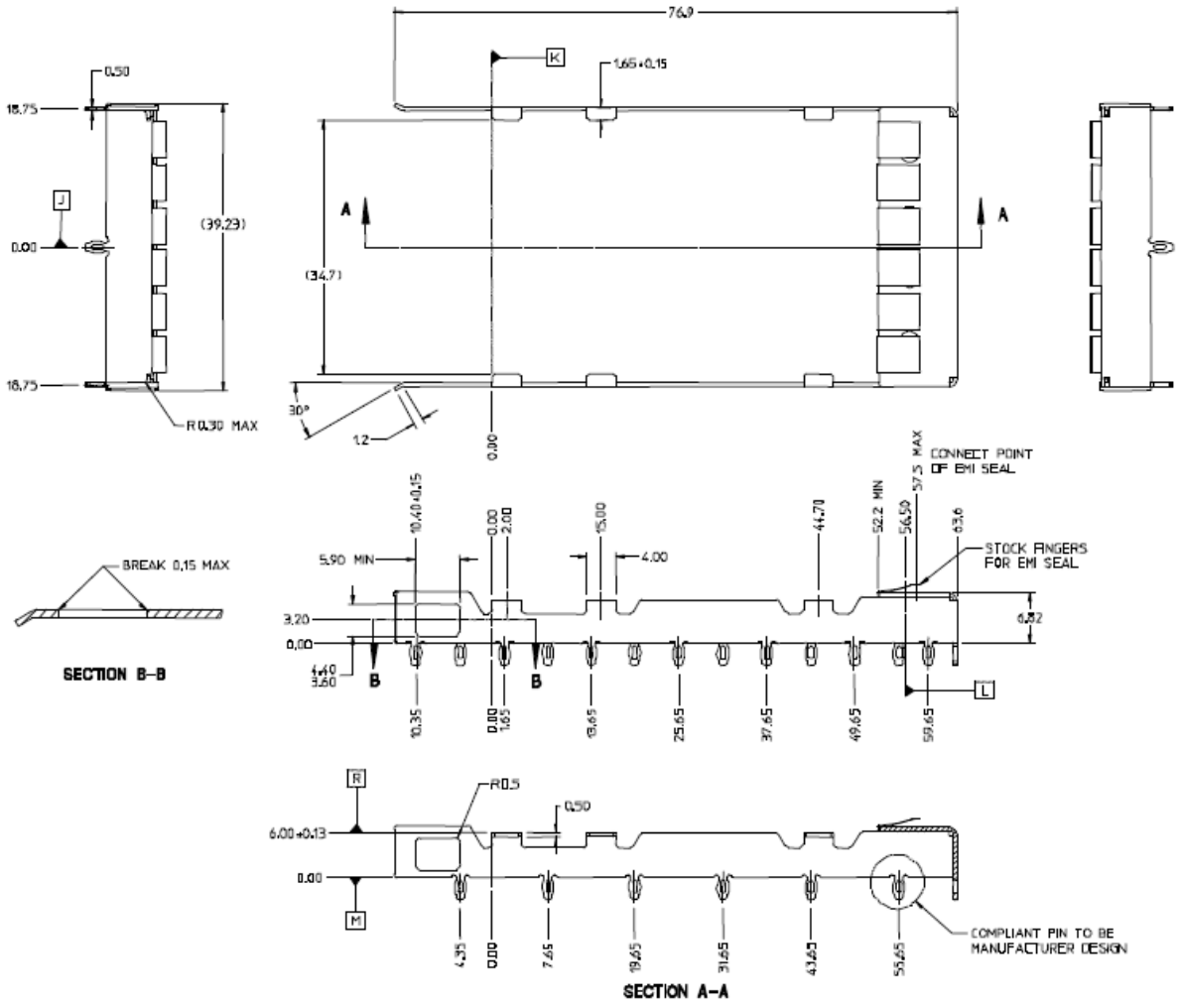

Figure 16 Mechanical dimensions on X2 rail

Table11 Definition of Datums

DATUM	DESCRIPTION TRANSCEIVER/RAIL
B	PHYSICAL HARD STOP ON TRANSCEIVER
C	INSIDE EDGE OF SLOT ON TRANSCEIVER
D	VERTICAL CENTER OF TRANSCEIVER PCB
E	TOP SURFACE OF SLOT ON TRANSCEIVER
F	FRONT SURFACE OF CUSTOMER'S FACE PLATE
J	INSIDE EDGE OF MOUNTING TABS ON RAIL
K	PHYSICAL HARD STOP ON RAIL
L	CENTER POF CONNESTOR LOCATION POINT ON CUSTOMER'S PCB
M	BOTTOM OF RAIL
R	TOP EDGE OF MOUNTING TABS ON RAIL

Optical Connector

No.	Parameter	Specifications	Remarks
1	SC Duplex Receptacle	IEC61754-4	Optical bores 12.25/13.15mm
2	SC Duplex plug	IEC61754-4	Optical bores 12.25/13.15mm

Electrical Connector

No.	Part name	Maker	Remarks
1	1367337-1or Equivalent	TycoAMP	70pin connector

Label location

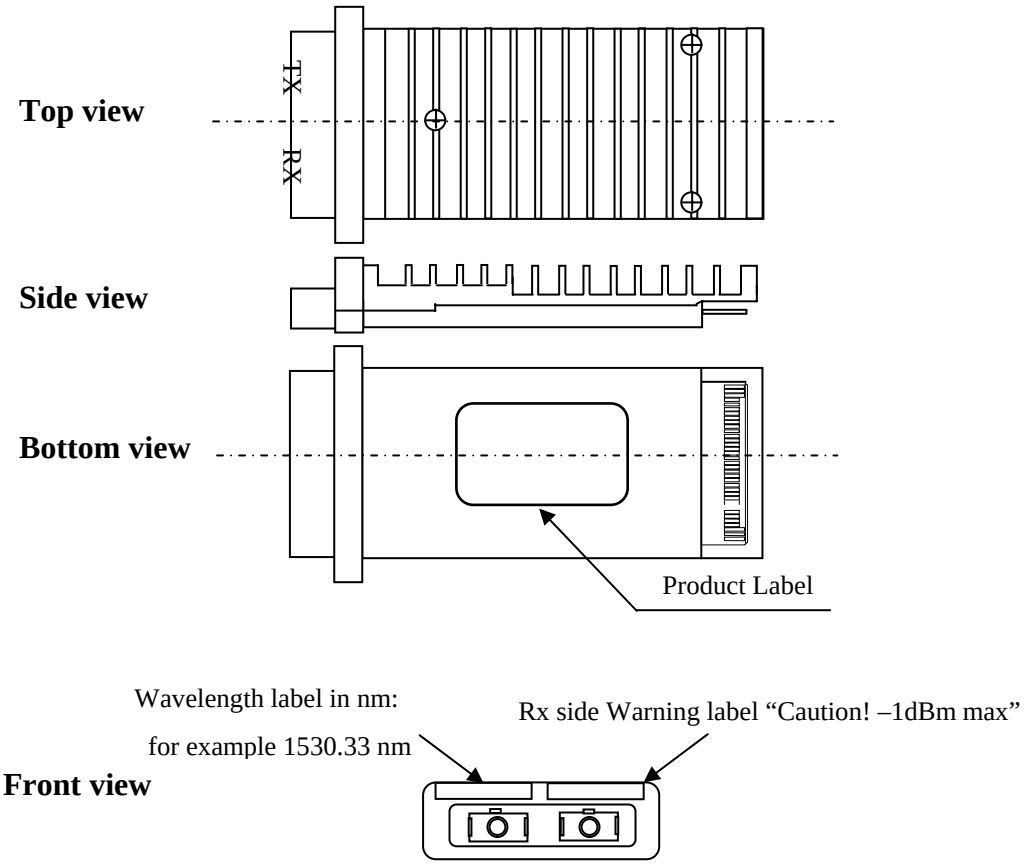

Figure 17 Labels location

Product Labels

The label contains the following information.
Opnext P/N, S/N, S/N barcode, Opnext Logo, Manufacture information, Laser classification, Lasing wavelength, ITU-T channel number.
The size is 15 x 35 mm.

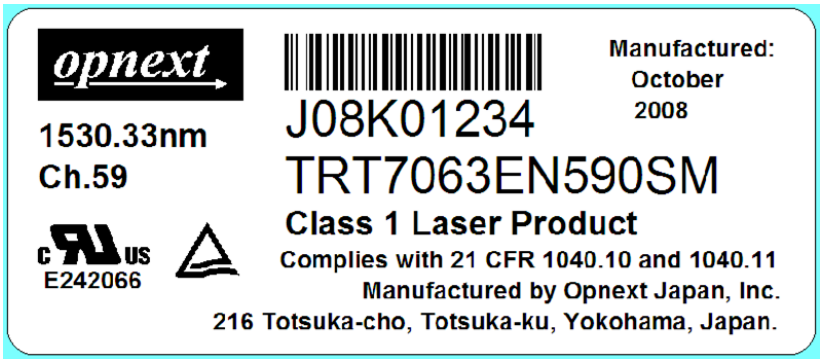

Figure 18 Product Label (Example of TRT7063EN590SM)

ORDERING INFORMATION

As stated in the disclaimer, the Opnext P/N will have the –F, –Fx, –W or –Wx at the end for functional samples and working samples.
For example: TRT7063ENabcSM-W

TRT 7 0 6 3 E N abc SM -W
(1) (2)(3)(4)(5)(6)(7) (8) (9) (10)

Item	Parameter	Symbol
(1) (2) (3) (4) (5)	Product Name	**TRT7063**: 10GBASE X2 ZR 80km 1550 nm EA-DFB / APD transceiver
(6) (7)	Product Code	**EN**: 10.3125Gbit/s and 10GbE Spec
(8)	Wavelength	**ab**=ITU-T ch number **c**=0 See table below
(9)	Custom Code	**SM**: General specification with mid height heat sink
(10)	Product Code	**Wn**: Working Sample (n:null or Version number of 2 and over is applied for this product) **Null**: Mass Production Product

ITU-T	Frequency	Wavelength	P/N
(ch)	(THz)	(nm)	
21	192.10	1560.61	TRT7063EN210SM
22	192.20	1559.79	TRT7063EN220SM
23	192.30	1558.98	TRT7063EN230SM
24	192.40	1558.17	TRT7063EN240SM
25	192.50	1557.36	TRT7063EN250SM
26	192.60	1556.55	TRT7063EN260SM
27	192.70	1555.75	TRT7063EN270SM
28	192.80	1554.94	TRT7063EN280SM
29	192.90	1554.13	TRT7063EN290SM
30	193.00	1553.33	TRT7063EN300SM
31	193.10	1552.52	TRT7063EN310SM
32	193.20	1551.72	TRT7063EN320SM
33	193.30	1550.92	TRT7063EN330SM
34	193.40	1550.12	TRT7063EN340SM
35	193.50	1549.32	TRT7063EN350SM
36	193.60	1548.51	TRT7063EN360SM
37	193.70	1547.72	TRT7063EN370SM
38	193.80	1546.92	TRT7063EN380SM
39	193.90	1546.12	TRT7063EN390SM
40	194.00	1545.32	TRT7063EN400SM
41	194.10	1544.53	TRT7063EN410SM
42	194.20	1543.73	TRT7063EN420SM
43	194.30	1542.94	TRT7063EN430SM
44	194.40	1542.14	TRT7063EN440SM
45	194.50	1541.35	TRT7063EN450SM
46	194.60	1540.56	TRT7063EN460SM
47	194.70	1539.77	TRT7063EN470SM
48	194.80	1538.98	TRT7063EN480SM
49	194.90	1538.19	TRT7063EN490SM
50	195.00	1537.40	TRT7063EN500SM
51	195.10	1536.61	TRT7063EN510SM
52	195.20	1535.82	TRT7063EN520SM
53	195.30	1535.04	TRT7063EN530SM
54	195.40	1534.25	TRT7063EN540SM
55	195.50	1533.47	TRT7063EN550SM
56	195.60	1532.68	TRT7063EN560SM
57	195.70	1531.90	TRT7063EN570SM
58	195.80	1531.12	TRT7063EN580SM
59	195.90	1530.33	TRT7063EN590SM

Document number: **OPN-DST-08032**

Document Category: Product Specifications (Data Sheet)
Revision: 0.0
Product Name: TRT7063ENabcSM-x

10GbE 80km DWDM-X2 Transceiver

TRT7063ENabcSM-x

Revision History

Rev.	Date	Page/Line/Fig/Table	Modification	Note
0.0	Dec. 5, 2008	-	-	Preliminary issue

X2 Transceiver MDIO Interface Registers

Parts Name	TRT7063EN-SM (STD) TRT7063ENabcSM (STD)

Reference documents

1) IEEE 802.3ae as 10GBASE-LR X2 MSA Release 2.0b

Table 1. Device Address

address	MMD name	Install
0	reserved	-
1	PMA/PMD	O
2	WIS	x
3	PCS	O
4	PHY XS	O
5	DTE XS	x
6 ~ 29	reserved	-
30	Vender spec.1	-
31	Vender spec.2	-

note

(*1)	If a register is defined with bit assignment, bit, names and descriptions of each bit are given in first second and third columns in the description of the register.
(*2)	Properties of register or bit: RO: Read Only, R/W: Read/Write, LH: Latch High, LL: Latch Low, RC: Read Clear and SC Self Cleaning.
(*3)	Initial Values are given in four Hexadecimal or one Binary numbers.

Table 2. PMA/PMD Registers (Device Address=1)

Add (hex)	Name	Description (*1)		(*2)	Initial (*3)	Description for Initial Value
0000	PMA/PMD Control 1	15	Reset	R/W	0	1: Reset, 0: Normal Operation
		14	reserved	RO	x	
		13	Speed Selection	RO	1	Operation at 10.3125 Gbit/s (All others are ignored)
		12	reserved	RO	x	
		11	Low Power	R/W	0	1: Low Power Mode, 0: Normal Operation (A reset is required to exit power down mode)
		10~7	reserved	RO	all x	
		6	Speed Selection	RO	1	Operation at 10.3125 Gbit/s (All others are ignored)
		5		RO	0	10 Gbit/s
		4		RO	0	(All others are ignored)
		3		RO	0	
		2		RO	0	
		1	reserved	RO	x	
		0	PMA Loop-back	R/W	0	1: Enable PMA loop-back mode, 0 : Disable
0001	PMA/PMD Status 1	15~8	reserved	RO	all x	
		7	Local Fault	RO	0	1: Local fault condition detected, 0 : not detected
		6~3	reserved	RO	all x	
		2	Receive Link Status	RO/LL	1	1: PMA locked to receive signal, 0 : not locked
		1	Low Power Ability	RO	1	PMA/PMD supports low power mode
		0	reserved	RO	x	
0002	Device Identifier	PMA/PMD Device Identifier		RO	0x0340	AEL1001; Returns contents of1.8036-1.8037
0003		OUI, Model No, and Rev No.		RO	0x0910	Returns contents of1.8038-1.8039
0004	Speed Ability	15~1	reserved	RO	all x	
		0	10G Capable	RO	1	PMA/PMD is capable of operating at 10G
0005	Devices in Package 1	15~6	reserved	RO	all x	
		5	DTE XS present	RO	0	DTE XS not present in package
		4	PHY XS present	RO	1	PHY XS present in package
		3	PCS present	RO	1	PCS present in package
		2	WIS present	RO	0	WIS not present in package
		1	PMA/PMD present	RO	1	PMA/PMD present in package
		0	Clause 22 registers present	RO	0	Clause 22 registers not present in package
0006	Devices in Package 2	15~14	Vendor-specific Device present	RO	all 0	Vendor specific device not present in package
		13~0	reserved	RO	all x	
0007	10G PMA/PMD Control 2	15~3	reserved	RO	all x	
		2		RO	0	TRT7063 is for 80km = Not specified in the standard
		1		RO	0	
		0	PMA/PMD Type Selection	RO	0	
0008	10G PMA/PMD Status 2	15		RO	1	Device responding at this address
		14	Device Present	RO	0	All other codes means no device responding at this address
		13	Transmit local fault ability	RO	1	1: Ability to detect local fault condition on transmit path
		12	Receive local fault ability	RO	1	1: Ability to detect local fault condition on receive path
		11	Transmit local fault	RO/LH	0	1: Local fault condition detected on transmit path, 0 : No local
		10	Receive local fault	RO/LH	0	1: Fault condition detected on receive path, 0 : No Fault
		9	reserved	RO	x	
		8	PMD transmit disable ability	RO	1	PMD has the ability to disable the transmit path
		7	10GBASE-SR ability	RO	0	PMA/PMD is not able to perform 10GBASE-SR
		6	10GBASE-LR ability	RO	0	PMA/PMD is not able to perform 10GBASE-LR
		5	10GBASE-ER ability	RO	0	PMA/PMD is not able to perform 10GBASE-ER
		4	10GBASE-LX4 ability	RO	0	PMA/PMD is not able to perform 10GBASE-LX4
		3	10GBASE-SW ability	RO	0	PMA/PMD is not able to perform 10GBASE-SW
		2	10GBASE-LW ability	RO	0	PMA/PMD is not able to perform 10GBASE-LW
		1	10GBASE-EW ability	RO	0	PMA/PMD is not able to perform 10GBASE-EW
		0	PMA loop-back ability	RO	1	Ability to perform PMA loop-back
0009	10G PMD Transmit	15~1	reserved	RO	all x	
		0	Global PMD transmit disable	R/W	0	1: Disable transmitter output, 0 : Enable
000A	10G PMD Receive Signal	15~1	reserved	RO	all x	
		0	Global PMD receive signal detect	RO	1	1: Signal detect on receive, 0: Signal not detect on receive
000B~000D		reserved			all x	
000E	Package Identifier	Package Identifier		RO	0x00C0	
000F		OUI Model No, and Rev No.		RO	0x9820	XENPAK OUI: 00-08-BE
0010~7FFF		reserved			all x	

Add (hex)	Name	Description (*1)		(*2)	Initial (*3)	Description for Initial Value
8000	Vender specific, EEPROM Control Register	15~9	reserved	RO	x	
		8	Low power initialization	RO	0	
		7,6	reserved	RO	x	
		5	Read/Write Command	R/W	x	1: Write mode, 0 : Read mode
		4	reserved	RO	x	
		3	Command Status	RO/LH	x	[3:2]=11: previous command failed [3:2]=10: command in progress
		2			x	[3:2]=01: command completed [3:2]=00: no command
		1	EEPROM command	R/W	x	[1:0]=11: read or write 256 bytes (default) [1:0]=10: reserved
		0			x	[1:0]=01: reserved [1:0]=00: reserved
8001~8006			reserved	RO	all x	
8007 ~ 8106	EEPROM register	15~8	reserved	**see Appendix A. NVR area**		
		7~0	NVR register 0~256			
8107~8FFF			extended vender specific and	RO	all x	
9000	LASI control and status, RX_ALARM Control	15~10	reserved	RO	all x	
		9	WIS_ENB	R/W	0	1: WIS Local Fault Enable, 0: Disable
		8~6	reserved	R/W	all x	
		5	Optical power Fault en	R/W	1	
		4	PMA/D_RX_FLT_ENB	R/W	1	1: PMA/PMD Receiver Local Fault Enable, 0 : Disable
		3	PCS_RX_FLT_ENB	R/W	1	1: PCS Receive Local Fault Enable, 0 : Disable
		2	reserved	R/W	x	
		1	RX flag enable	R/W	0	1: RX Flag Enable, 0 : Disable
		0	XS_RX_FLT_ENB	R/W	1	1: PHY XS Receive Local Fault Enable, 0 : Disable
9001	TX_ALARM Control	15~10	reserved	RO	all x	
		9	Laser Bias En	RO	1	
		8	Laser Temp En	RO	1	
		7	Laser Power En	RO	1	
		6	TX_FLT_ENB	RO	1	1: Transmitter Fault Enable, 0 : Disable (1: MSA Mode)
		5	reserved	RO	x	
		4	PMA/D_TX_FLT_ENB	RO	1	1: PMA/PMD Transmitter Local Fault Enable, 0 : Disable
		3	PCS_TX_FLT_ENB	RO	1	1: PCS Transmit Local Fault Enable, 0 : Disable
		2	reserved	RO	x	
		1	TX_FLAG_ENB	RO	0	1: TX Flag Enable, 0 : Disable
		0	XS_TX_FLT_ENB	RO	1	1: PHY XS Transmit Local Fault Enable, 0 : Disable
9002	LASI Control	15~6	reserved	RO	all x	
		5	V3_3err_EN	R/W	0	3.3-V Out of spec enable.
		4	V1_2err EN	R/W	0	1.2-V Out of spec enable.
		3	reserved	RO	x	
		2	RX_AM_ENB	R/W	0	1: Receiver alarm enable, 0 : disable
		1	TX_AM_ENB	R/W	0	1: Transmitter alarm enable, 0 : disable
		0	LS_AM _ENB	R/W	0	1: Link Status alarm enable, 0 : disable
9003	RX_ALARM Status	15~10	reserved	RO	all x	
		9	WIS fault	RO	0	WIS Local Fault.
		8~6	reserved	RO	all x	
		5	Optical power fault	RO/LH	0	1: Fault detected, 0 : not detected (RC/LH: MSA Mode)
		4	PMA/D_RX_FLT	RO/LH	0	1: PMA/PMD Receiver Local Fault detected, 0 : not detected
		3	PCS_RX_FLT	RO/LH	0	1: PCS Receive Local Fault detected, 0 : not detected
		2	reserved	RO	x	
		1	RX_ALM_FLAG	RO/LH	0	Set if 0xA071 bit 6 or 7 and corresponding enable bit in 0x9007 are set (RC/LH: MSA Mode)
		0	XS_RX _FLT	RO/LH	0	1: PHY XS Receive Local Fault detected, 0 : not detected
9004	TX_ALARM Status	15~10	reserved	RO	x	
		9	Laser Bias	RO/LH	0	1: Fault detected, 0 : not detected (RC/LH: MSA Mode)
		8	Laser Temp	RO/LH	0	1: Fault detected, 0 : not detected (RC/LH: MSA Mode)
		7	Laser Power	RO/LH	0	1: Fault detected, 0 : not detected (RC/LH: MSA Mode)
		6	TX Fault	RO/LH	0	1: Transmitter Fault detected, 0 : not detected
		5	reserved	RO	x	
		4	PMA/D_TX_FLT	RO/LH	0	1: PMA/PMD Transmit Local Fault detected, 0 : not detected
		3	PCS_TX_FLT	RO/LH	0	1: PCS Transmit Local Fault detected, 0 : not detected
		2	reserved	RO	x	
		1	TX_ALM_FLAG	RO/LH	0	Set if 0xA070 and corresponding enable bit in 0x9006 are set (RC/LH: MSA
		0	XS_TX _FLT	RO/LH	0	1: PHY XS Transmit Local Fault detected, 0 : not detected
9005	LASI Status	15~6	reserved	RO	all x	
		5	V3_3err	RO	0	3.3-V Supply out of range
		4	V1_2err	RO	0	1.2-V Supply out of range
		3	reserved	RO	x	
		2	RX_ALARM	RO	0	1: Receiver alarm condition occurred, 0 : not occurred
		1	TX_ALARM	RO	0	1: Transmitter alarm condition occurred, 0 : not occurred
		0	LS_ALARM	RO/LH	0	1: Link Status alarm condition occurred, 0 : not occurred
9006	TX_FLAG Control Bits	15~8	reserved	RO	all x	
		7	TCVR_T_H_ALM_ENABLE	R/W	0	1: Transceiver temp High Alarm Enable, 0 : Disable
		6	TCVR_T_L_ALM_ENABLE	R/W	0	1: Transceiver temp Low Alarm Enable, 0 : Disable
		5,4	reserved	RO	all x	
		3	LBC_H_ ALM_ENABLE	R/W	0	1: Laser Bias Current High Alarm Enable, 0 : Disable
		2	LBC_L_ ALM_ENABLE	R/W	0	1: Laser Bias Current Low Alarm Enable, 0 : Disable
		1	LOP_H_ALM_ENABLE	R/W	0	1: Laser Output power High Alarm Enable, 0 : Disable
		0	LOP_L_ALM_ENABLE	R/W	0	1: Laser Output power Low Alarm Enable, 0 : Disable
9007	RX_FLAG Control Bits	15~8	reserved	RO	all x	
		7	ROP_H_ALM_ENABLE	R/W	0	1: Receive Optical power High Alarm Enable, 0 : Disable
		6	ROP_L_ALM_ENABLE	R/W	0	1: Receive Optical power Low Alarm Enable, 0 : Disable
		5~0	reserved	RO	all x	
9008~9FFF			reserved			

Add (hex)	Name	Description (*1)		(*2)	Initial (*3)	Description for Initial Value
A000	EEPROM	15~8	reserved	**see Appendix B. Alarm and Warning**		
~ A05FF	register	7~0	NVR register 0~95			
A060	Transceiver	MSB at low address		RO	x	Temperature accuracy is +/-5 degree C over specified operating temperature and voltage.
A061	Temp	LSB : 1/256 degC		RO	x	
A062		MSB at low address		RO	x	Accuracy is +/-10 % of the Opnext set-point over specified operation temperature and voltage.
A063	Vcc monitor	LSB : 0.1mV		RO	x	
A064	Laser Bias	MSB at low address		RO	x	Accuracy is +/-10 % of the Opnext set-point over specified operation temperature and voltage.
A065	Current	LSB : 0.2uV		RO	x	
A066	Laser Output	MSB at low address		RO	x	Accuracy is +/-3 dB over average transmit power range, from -1 to 3 dBm.
A067	Power	LSB : 0.1uW		RO	x	
A068	Recive Optical	MSB at low address		RO	x	Accuracy is +/-3 dB over average receive power range, from –24 to -7 dBm.
A069	Power	LSB : 0.1uW		RO	x	
A06A~A06D			reserved	RO	all 0	
		15~8	reserved	RO	all x	
		7	IND_TX_TEM_M_C	R/W	1	Set to indicate transceiver temperature monitoring capable
		6	IND_LD_BIAS_M_C	R/W	1	Set to indicate laser bias current monitoring capable
		5	IND_LD_PWR_M_C	R/W	1	Set to indicate laser output power monitoring capable
		4	IND_RX_PWR_M_C	R/W	1	Set to indicate receive optical power monitoring capable
		3	IND_ALM_FLG	R/W	1	Set to indicate alarm flags implemented for monitored quantities
		2	IND_WRN_FLG	R/W	1	Set to indicate warning flags implemented for monitored quantities
	DOM Capability	1	IND_LASI_FLG	R/W	1	Set to indicate LASI fanction inputs implemented for monitored quantities
A06F	Extended	0	reserved	RO	x	
		15~8	reserved	RO	all x	
		7	TCVR_T_H_ALM	RO/LH	0	1: Transceiver Temp High Alarm condition occurred, 0 : not occurred (RO:
		6	TCVR_T_L_ALM	RO/LH	0	1: Transceiver Temp Low Alarm condition occurred, 0 : not occurred (RO:
		5,4	reserved	RO	all x	
		3	LBC_H_ALM	RO	0	1: Laser Bias Current High Alarm condition occurred, 0 : not occurred (RO: MSA Mode)
		2	LBC_L_ALM	RO	0	1: Laser Bias Current Low Alarm condition occurred, 0 : not occurred (RO: MSA Mode)
		1	LOP_H_ALM	RO	0	1: Laser Output Power High Alarm condition occurred, 0 : not occurred (RO: MSA Mode)
	TX_ALARM_FL					
A070	AG Bits	0	LOP_L_ALM	RO	0	1: Laser Output Power Low Alarm condition occurred, 0 : not occurred (RO: MSA Mode)
		15~8	reserved	RO	all x	
		7	ROP_H_ALM	RO	0	1: Receive Optical Power High Alarm condition occurred, 0 : not occurred (RO: MSA Mode)
	RX_ALARM_FL	6	ROP_L_ALM	RO	0	1: Receive Optical Power Low Alarm condition occurred, 0 : not occurred (RO: MSA Mode)
A071	AG Bits	5~0	reserved	RO	all x	
		15~8	reserved	RO	all x	
		7	TCVR_T_H_WARN	RO	0	1: Transceiver Temp High Warning condition occurred, 0 : not occurred
		6	TCVR_T_L_WARN	RO	0	1: Transceiver Temp Low Warning condition occurred, 0 : not occurred
		5,4	reserved	RO	all x	
		3	LBC_H_WARN	RO	0	1: Laser Bias Current High Warning condition occurred, 0 : not occurred
		2	LBC_L_WARN	RO	0	1: Laser Bias Current Low Warning condition occurred, 0 : not occurred
	TX_WARNING_	1	LOP_H_WARN	RO	0	1: Laser Output Power High Warning condition occurred, 0 : not occurred
A074	FLAG Bits	0	LOP_L_WARN	RO	0	1: Laser Output Power Low Warning condition occurred, 0 : not occurred
		15~8	reserved	RO	all x	
		7	ROP_H_WARN	RO	0	1: Receive Optical Power High Warning condition occurred, 0 : not
	RX_WARNING_	6	ROP_L_WARN	RO	0	1: Receive Optical Power Low Warning condition occurred, 0 : not occurred
A075	FLAG Bits	5~0	reserved	RO	all x	
A076~A0FF			reserved			
		15~4	reserved	RO	all x	
		3		RO/LH	0	00: Idle 01: Command completed successfully
		2	Command Status		0	10: Command in progress 11: Command failed
		1		R/W	0	00: Write to bits initiates a single update of MDIO registers with all bytes of DOM information. Write of this bit combination also stops periodic update modes. 01: Write to bits initiates a periodic update of MDIO registers with all bytes of DOM information. Frequency of update is vendor specific, but this bit combination provides the slowest rate of periodic update.
	OPTICAL_DOM	0	Update Commands		0	10: Write to bits initiates a periodic update of MDIO registers with all bytes of DOM information. Frequency of update is vendor specific, but this bit combination provides the intermediate rate of periodic update. 11: Write to bits initiates a periodic update of MDIO registers with all bytes of DOM information. Frequency of update is vendor specific, but this bit combination provides the fastest rate of periodic update.
A100	Control/Status					
A101~FFFF			Vender specific		all x	

Table 3. PCS Registers (Device Address= 3)

Add (hex)	Name	Description (*1)		(*2)	Initial (*3)	Description for Initial Value
		15	Reset	R/W	0	1: Reset, 0: Normal Operation
		14	Loop-back	R/W	0	1: Enable PCS system loop-back mode, 0: Disable
		13	Speed Selection	RO	1	Operation at 10.3125 Gbit/s (All others are ignored)
		12	reserved	RO	x	
		11	Low Power	R/W	0	1: Low Power Mode, 0: Normal Operation (A reset is required to exit power down mode)
		10~7	reserved	RO	all x	
		6	Speed Selection	RO	1	Operation at 10.3125 Gbit/s (All others are ignored)
		5		RO	0	10 Gbit/s
		4		RO	0	(All others are ignored)
		3		RO	0	
		2		RO	0	
0000	PCS Control 1	1,0	reserved	RO	all x	
		15~8	reserved	RO	all x	
		7	Local Fault	RO	0	1: Local fault detected, 0 : Not detected
		6~3	reserved	RO	all x	
		2	PCS receive link status	RO/LL	1	1: PCS receive link up, 0: PCS receive link down
		1	Low Power ability	RO	1	Always returns1.
0001	PCS Status 1	0	reserved	RO	x	
0002		PCS Device Identifier		RO	0x0340	Returns contents of 1.8036-8037.
0003	Device Identifier	OUI, Model No, and Rev No.		RO	0x0910	Returns contents of 1.8038-8039.
		15~1	reserved	RO	all x	
0004	Speed Ability	0	10G Capable	RO	1	Returns 1.
		15~6	reserved	RO	all x	
		5	DTE XS present	RO	0	DTE XS not present in package
		4	PHY XS present	RO	1	PHY XS present in package
		3	PCS present	RO	1	PCS present in package
		2	WIS present	RO	0	WIS not present in package
	Devices in	1	PMD/PMA present	RO	1	PMD/PMA present in package
0005	Package 1	0	Clause 22 registers present	RO	0	Clause 22 registers not present in package
	Devices in	15~14	Vendor-specific Device present	RO	all 0	Returns 00.
0006	Package 2	13~0	reserved	RO	all x	
		15~2	reserved	RO	all x	
		1		RO	0	10GBASE-R PCS type
0007	PCS Control 2	0	PCS Type Selection	RO	0	(Not specified in the standard)
		15		RO	1	Device responding at this address
		14	Device Present	RO	0	All other codes means no device responding at this address
		13,12	reserved	RO	all x	
		11	Transmit local fault	RO/LH	0	1: Local fault condition on transmit path, 0 : No fault
		10	Receive local fault	RO/LH	0	1: Local fault condition on transmit path, 0 : No fault
		9~3	reserved	RO	all x	
		2	10GBASE-W capable	RO	0	PCS is not able to support 10GBASE-W PCS type
		1	10GBASE-X capable	RO	0	PCS is not able to support 10GBASE-X PCS type
0008	PCS Status 2	0	10GBASE-R capable	RO	1	PCS is able to support 10GBASE-R PCS type
0009~001F			reserved		all x	
		15~13	reserved	RO	all x	
		12	10GBASE-R Receive link status	RO	0	1: 10GBASE-R PCS receive link up, 0 : link down
		11~3	reserved	RO	all x	
		2	PRBS Pattern testing ability	RO	1	PCS is able to support PRBS31 pattern testing
	10GBASE-R	1	10GBASE-R PCS high BER	RO	0	1: 10GBASE-R PCS reporting a high BER, 0 : not reporting
0020	PCS Status 1	0	10GBASE-R PCS block	RO	0	1: 10GBASE-R PCS locked to received blocks, 0 : not locked
		15	Latched block lock	RO/LL	0	1: 10GBASE-R PCS has block lock, 0 : not lock
		14	Latched high BER	RO/LH	0	1: 10GBASE-R PCS has reported a high BER, 0 : not reported
	10GBASE-R	13~8	BER	RO	0	BER Counter
0021	PCS Status 2	7~0	Errored blocks	RO	0x00	Errored blocks counter
0022			Test pattern seed A0	RW	AAAA	Test pattern seed A bits 0-15
0023			Test pattern seed A1	RW	AAAA	Test pattern seed A bits 16-31
0024	10GBASE-R		Test pattern seed A2	RW	AAAA	Test pattern seed A bits 32-47
	PCS Test	15~10	reserved	RO	all x	
0025	pattern Seed	9~0	Test pattern seed A3	RW	2AA	Test pattern seed A bits 48-57
0026			Test pattern seed B0	RW	AAAA	Test pattern seed B bits 0-15
0027			Test pattern seed B1	RW	AAAA	Test pattern seed B bits 16-31
0028	10GBASE-R		Test pattern seed B2	RW	AAAA	Test pattern seed B bits 32-47
	PCS Test	15~10	reserved	RO	all x	
0029	pattern Seed	9~0	Test pattern seed B3	RW	2AA	Test pattern seed B bits 48-57
		15~6	reserved	RO	all x	
		5	PRBS 31 Receive test pattern	RW	0	1: Enable PRBS 31 test pattern mode on receive path, 0 : Disable
		4	PRBS 31 Transmit test pattern	RW	0	1: Enable PRBS 31 test pattern mode on transmit path, 0 : Disable
		3	Tansmit test pattern enable	RW	0	1: Enable transmit test pattern. 0 : Disable
	10GBASE-R	2	Receive test pattern enable	RW	0	1: Enable receive test pattern testing. 0 : Disable
	PCS Test	1	Test pattern select	RW	0	1: Square wave test pattern, 0: Pseudo-random test pattern
002A	pattern Conotrol	0	Data pattern select	RW	0	1: Zeros data pattern, 0: LF data pattern
002B	Error Counter	Test		RO	0	Error counter
002C~7FFF			reserved		all x	
8000~FFFF			Vender specific		all x	

Table 4. PHY XS Registers (Device Address= 4)

Add (hex)	Name	Description (*1)		(*2)	Initial (*3)	Description for Initial Value
0000	PHY XS Control 1	15	Reset	R/W	0	1: Reset, 0: Normal Operation
		14	Loop-back	R/W	0	1: Enable XGXS loop-back mode, 0: Disable
		13	Speed Selection	RO	1	Operation at 10.3125 Gbit/s (All others are ignored)
		12	reserved	RO	x	
		11	Low Power	R/W	0	1: Low Power Mode, 0: Normal Operation (A reset is required to exit power down mode)
		10~7	reserved	RO	all x	
		6	Speed Selection	RO	1	Operation at 10.3125 Gbit/s (All others are ignored)
		5	Speed Selection	RO	0	10 Gbit/s (All others are ignored)
		4		RO	0	
		3		RO	0	
		2		RO	0	
		1,0	reserved	RO	all x	
0001	PHY XS Status 1	15~8	reserved	RO	all x	
		7	Local Fault	RO	0	1: Local fault detected, 0 : Not detected
		6~3	reserved	RO	all 0	
		2	PHY XS Transmit link status	RO/LL	1	1: PHY XS transmit link is up, 0: PHY XS transmit link is down
		1	Low Power ability	RO	1	PHY XS supports low power mode
		0	reserved	RO	x	
0002	Device Identifier	PHY XS Device Identifier		RO	0x0340	Returns contents of 1.8036-8037.
0003		OUI, Model No, and Rev No.		RO	0x0910	Returns contents of 1.8038-8039.
0004	Speed Ability	15~1	reserved	RO	all x	
		0	10G Capable	RO	1	PHY XS is capable of operating at 10G
0005	Devices in Package 1	15~6	reserved	RO	all x	
		5	DTE XS present	RO	0	DTE XS not present in package
		4	PHY XS present	RO	1	PHY XS present in package
		3	PCS present	RO	1	PCS present in package
		2	WIS present	RO	0	WIS not present in package
		1	PMD/PMA present	RO	1	PMD/PMA present in package
		0	Clause 22 registers present	RO	0	Clause 22 registers not present in package
0006	Devices in Package 2	15~14	Vendor-specific Device present	RO	all 0	Vendor-specific device not present in package
		13~0	reserved	RO	all x	
0007			reserved		all 0	
0008	PHY XS Status 2	15	Device Present	RO	1	Device responding at this address
		14		RO	0	All other codes means no device responding at this address
		13,12	reserved	RO	all x	
		11	Transmit local fault	RO/LH	0	1: Local fault detected on transmit path, 0 : No local fault
		10	Receive local fault	RO/LH	0	1: Local fault detected on receive path, 0 : No local fault
		9~0	reserved	RO	all x	
0009~000D			reserved		all x	
000E	PHY Identifier	15~0	PHY XS Package Identifier	RO	0x0000	Returns 0.
000F	PHY Identifier	15~0	PHY XS Package Identifier	RO	0x0000	Returns 0.
0010~0017			reserved		all x	
0018	10G PHY XGXS Lane Status	15~13	reserved	RO	all x	
		12	XGXS lane alignment status	RO	0	1: PHY XGXS transmit lanes aligned, 0 : not aligned
		11	Pattern testing ability	RO	0	PHY XGXS is able to generate test patterns
		10	PHY XGXS loop-back ability	RO	1	Capable of XGXS loop-back
		9~4	reserved	RO	all x	
		3	Lane 3 sync	RO	0	1: XAUI Lane 3 is synchronized, 0 : Not synchronized
		2	Lane 2 sync	RO	0	1: XAUI Lane 2 is synchronized, 0 : Not synchronized
		1	Lane 1 sync	RO	0	1: XAUI Lane 1 is synchronized, 0 : Not synchronized
		0	Lane 0 sync	RO	0	1: XAUI Lane 0 is synchronized, 0 : Not synchronized
0019	10G PHY XGXS Test Control	15~3	reserved	RO	all x	
		2	Receive test pattern enable	RO	0	1: Receive test pattern enabled, 0: Not enabled
		1	Test pattern select	RO	0	[1:0]=11: Reserved [1:0]=10: Mixed-frequency test pattern
		0			0	[1:0]=01: Low-frequency test pattern [1:0]=00: High-frequency test pattern
001A~7FFF			reserved		all x	
8000~FFFF			Vender specific		all x	

Appendix A-3. NVR area [TRT7063ENabcSM]

0x8000	NVR Control Status
0x8001 - 0x8006	Vendor Specific
0x8007 - 0x8106	Non-volatile Registers
0x8107 - 0x8806	Extended vendor specific Non-volatile area
0x8807 - 0x8FFF	Reserved

type : A = All Opnext X2 common
B = Parts Group (TRT7063EN) common
C = Parts name common (each wavelength peculiar)
D = Each parts (each serial number) peculiar
[Value of under table type C and D are for example]

Fields Group	hex	NVR Byte #	Size	Name	Description	Value	hex	type	Value	hex	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	note
Header	8007	0	1	Version	X2 MSA version			B	rev2.0	14	0	0	0	1	0	1	0	0	
	8008	1	2	NVR_Size	NVR Size in bytes			B	256 byte	01	0	0	0	0	0	0	0	1	
	8009	2								00	0	0	0	0	0	0	0	0	
	800A	3	2	Mem_Used	# of bytes used			B	256 byte	01	0	0	0	0	0	0	0	1	
	800B	4								00	0	0	0	0	0	0	0	0	
	800C	5	1	Basic Addr	Basic Field Address			B	start 11d	0B	0	0	0	0	1	0	1	1	
	800D	6	1	Cust Addr	Customer Field Address			B	start 119d	77	0	1	1	1	0	1	1	1	
	800E	7	1	Vend Addr	Vendor Field Address			B	start 167d	A7	1	0	1	0	0	1	1	1	
	800F	8	2	Ext Vend Addr	Extended Vendor Field Address			B	start 256d	01	0	0	0	0	0	0	0	1	
	8010	9								00	0	0	0	0	0	0	0	0	
	8011	10	1	Reserved						00	0	0	0	0	0	0	0	0	
Basic	8012	11	1	Tcvr Type	Transceiver Type	Unspecified	0	A	X2	02	0	0	0	0	0	0	1	0	
						X2	2												
	8013	12	1	Connector	Optical connector type	Unspecified	0	A	SC	01	0	0	0	0	0	0	0	1	
						SC	1												
						LC	2												
						MT-RJ	4												
						MU	8												
						FC/PC	10												
						Pigtail	20												
	8014	13	1	Encoding	Bit encoding	Unspecified	0	B	NRZ	01	0	0	0	0	0	0	0	1	
						NRZ	1												
						FEC	2												
	8015	14	2	Bit Rate	Nominal Bit Rate in Mb/s			B	10.3125=	28	0	0	1	0	1	0	0	0	
	8016	15							2848h	48	0	1	0	0	1	0	0	0	
	8017	16	1	Protocol	Protocol Type	Unspecified	0	B	10GbE	01	0	0	0	0	0	0	0	1	
						10GbE	1												
						10GFC	2												
						WIS	4												
						LSS	8												
						Sonet/SDH	10												
	8018	17	10	Standards Compliance Codes	10GbE Code byte 0	Unspecified	0	B	Unspecified	00	0	0	0	0	0	0	0	0	
						10GBASE-SR	1												
						10GBASE-LR	2												
						10GBASE-ER	4												
						10GBASE-LX4	8												
						10GBASE-SW	10												
						10GBASE-LW	20												
						10GBASE-EW	40												
	8019	18			10GbE Code byte 1	Reserved		A	Unspecified	00	0	0	0	0	0	0	0	0	
	801A	19			Sonet/SDH Code Byte 0	Unspecified	0	B	Unspecified	00	0	0	0	0	0	0	0	0	
						S-64.1	1												
						S-64.2a	2												
						S-64.2b	4												
						S-64-3a	8												
						S-64.3b	10												
						S-64.5a	20												
						S-64.5b	40												
	801B	20			Sonet/SDH Code Byte 1	Unspecified	0	B	Unspecified	00	0	0	0	0	0	0	0	0	
						I-64.1r	1												
						I-64.1	2												
						I-64.2r	4												
						I-64.2	8												
						I-64.3	10												
						I-64.5	20												
	801C	21			Sonet/SDH Code Byte 2	Unspecified	0	B	Unspecified	00	0	0	0	0	0	0	0	0	
						L-64.1	1												
						L-64.2a	2												
						L-64.2b	4												
						L-64.2c	8												
						L-64.3	10												
	801D	22			Sonet/SDH Code Byte 3	Unspecified	0	B	Unspecified	00	0	0	0	0	0	0	0	0	
						V-64.2a	1												
						V-64.2b	2												
						V-64.3	4												
	801E	23			10GFC Code byte 0	Reserved		A	Unspecified	00	0	0	0	0	0	0	0	0	
	801F	24			10GFC Code byte 1	Reserved		A	Unspecified	00	0	0	0	0	0	0	0	0	
	8020	25			10GFC Code byte 2	Reserved		A	Unspecified	00	0	0	0	0	0	0	0	0	
	8021	26			10GFC Code byte 3	Reserved		A	Unspecified	00	0	0	0	0	0	0	0	0	
	8022	27	2	Range	Transmission range in 10m			B	8000=	1F	0	0	0	1	1	1	1	1	
	8023	28							1F40h	40	0	1	0	0	0	0	0	0	
	8024	29	2	Fiber	Fiber Type byte 0	Unspecified	0	B	SM, generic	20	0	0	1	0	0	0	0	0	
						MM, generic	1												
						50/125 only	2												
						62.5/125 only	4												
						POF	8												
						HPCF	10												
						SM, generic	20												
						NDSF only	40												
						NZDSF only	80												
	8025	30			Fiber Type byte 1	Unspecified	0	B	Unspecified	00	0	0	0	0	0	0	0	0	
						Large core only	1												
						PMF only	2												
	8026	31	3	Wavelength chan 0	Center wavelength in 0.01nm steps - Channel 0			C	1550.00nm	02	0	0	0	0	0	0	1	0	
	8027	32								5D	0	1	0	1	1	1	0	1	
	8028	33								78	0	1	1	1	1	0	0	0	
	8029	34	3	Wavelength chan 1	Center wavelength in 0.01nm steps - Channel 1			B	Unspecified	00	0	0	0	0	0	0	0	0	
	802A	35							Unspecified	00	0	0	0	0	0	0	0	0	
	802B	36							Unspecified	00	0	0	0	0	0	0	0	0	
	802C	37	3	Wavelength chan 2	Center wavelength in 0.01nm steps - Channel 2			B	Unspecified	00	0	0	0	0	0	0	0	0	
	802D	38							Unspecified	00	0	0	0	0	0	0	0	0	
	802E	39							Unspecified	00	0	0	0	0	0	0	0	0	
	802F	40	3	Wavelength chan 3	Center wavelength in 0.01nm steps - Channel 3			B	Unspecified	00	0	0	0	0	0	0	0	0	
	8030	41							Unspecified	00	0	0	0	0	0	0	0	0	
	8031	42							Unspecified	00	0	0	0	0	0	0	0	0	
	8032	43	4	Package OUI	Package identifier in OUI	X2 OUI=		A	NVR Dev.= 1	00	0	0	0	0	0	0	0	0	**X2 MSA rev2.0**
	8033	44				000C64				C0	1	1	0	0	0	0	0	0	**000C64=>00, C0, 98, 20**
	8034	45								98	1	0	0	1	1	0	0	0	
	8035	46								20	0	0	1	0	0	0	0	0	
	8036	47	4	Vendor OUI	Transceiver vendor OUI	Opnext OUI=		B	**Model = 11**	03	0	0	0	0	0	0	1	1	**X2 MSA rev2.0**
	8037	48				000B40 0340091x			**Rev. = 00**	40	0	1	0	0	0	0	0	0	
	8038	49								09	0	0	0	0	1	0	0	1	**for Rev.**
	8039	50								10	0	0	0	1	0	0	0	0	

Fields Group	hex	NVR Byte #	Size	Name	Description	Value	hex	type	Value	hex	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	note
Basic	803A	51	16	Vendor Name	Transceiver vendor name in ASCII	OPNEXT,INC		A	**O**	4F	0	1	0	0	1	1	1	1	Opnext, Inc.
	803B	52							**p**	70	0	1	1	1	0	0	0	0	
	803C	53							**n**	6E	0	1	1	0	1	1	1	0	
	803D	54							**e**	65	0	1	1	0	0	1	0	1	
	803E	55							**x**	78	0	1	1	1	1	0	0	0	
	803F	56							**t**	74	0	1	1	1	0	1	0	0	
	8040	57							**,**	2C	0	0	1	0	1	1	0	0	
	8041	58							**I**	49	0	1	0	0	1	0	0	1	
	8042	59							**n**	6E	0	1	1	0	1	1	1	0	
	8043	60							**c**	63	0	1	1	0	0	0	1	1	
	8044	61							.	2E	0	0	1	0	1	1	1	0	
	8045	62								20	0	0	1	0	0	0	0	0	
	8046	63								20	0	0	1	0	0	0	0	0	
	8047	64								20	0	0	1	0	0	0	0	0	
	8048	65								20	0	0	1	0	0	0	0	0	
	8049	66								20	0	0	1	0	0	0	0	0	
	804A	67	16	Vendor PN	Part number from vendor in ASCII	**Opnext PN**		C	**T**	54	0	1	0	1	0	1	0	0	For example
	804B	68							**R**	52	0	1	0	1	0	0	1	0	TRF7063EN590SM
	804C	69							**T**	54	0	1	0	1	0	1	0	0	
	804D	70							**7**	37	0	0	1	1	0	1	1	1	
	804E	71							**0**	30	0	0	1	1	0	0	0	0	
	804F	72							**6**	36	0	0	1	1	0	1	1	0	
	8050	73							**3**	33	0	0	1	1	0	0	1	1	
	8051	74							**E**	45	0	1	0	0	0	1	0	1	
	8052	75							**N**	4E	0	1	0	0	1	1	1	0	
	8053	76							**5**	35	0	0	1	1	0	1	0	1	
	8054	77							**9**	39	0	0	1	1	1	0	0	1	
	8055	78							**0**	30	0	0	1	1	0	0	0	0	
	8056	79							**S**	53	0	1	0	1	0	0	1	1	
	8057	80							**M**	4D	0	1	0	0	1	1	0	1	
	8058	81								20	0	0	1	0	0	0	0	0	
	8059	82								20	0	0	1	0	0	0	0	0	
	805A	83	2	Vendor Rev	Revision level of PN in ASCII	Rev. 00		B	0	30	0	0	1	1	0	0	0	0	Rev
	805B	84							0	30	0	0	1	1	0	0	0	0	
	805C	85	16	Vendor SN	Vendor SN in ASCII			D	J	4A	0	1	0	0	1	0	1	0	for example
	805D	86							0	30	0	0	1	1	0	0	0	0	J08E12345
	805E	87							8	38	0	0	1	1	1	0	0	0	J: Made in Japan
	805F	88							E	45	0	1	0	0	0	1	0	1	08: CY 2008
	8060	89							1	31	0	0	1	1	0	0	0	1	E: Month ABCDEFGHJKLM
	8061	90							2	32	0	0	1	1	0	0	1	0	12345: S/N
	8062	91							3	33	0	0	1	1	0	0	1	1	
	8063	92							4	34	0	0	1	1	0	1	0	0	
	8064	93							5	35	0	0	1	1	0	1	0	1	
	8065	94								20	0	0	1	0	0	0	0	0	
	8066	95								20	0	0	1	0	0	0	0	0	
	8067	96								20	0	0	1	0	0	0	0	0	
	8068	97								20	0	0	1	0	0	0	0	0	
	8069	98								20	0	0	1	0	0	0	0	0	
	806A	99								20	0	0	1	0	0	0	0	0	
	806B	100								20	0	0	1	0	0	0	0	0	
	806C	101	4	Date Code	Vendor manufacturing date code in ASCII	Year		D	2	32	0	0	1	1	0	0	1	0	for example
	806D	102							0	30	0	0	1	1	0	0	0	0	2008
	806E	103							0	30	0	0	1	1	0	0	0	0	
	806F	104							8	38	0	0	1	1	1	0	0	0	
	8070	105	2			Month		D	0	30	0	0	1	1	0	0	0	0	May
	8071	106							5	35	0	0	1	1	0	1	0	1	
	8072	107	2			Day		D	1	31	0	0	1	1	0	0	0	1	15
	8073	108							5	35	0	0	1	1	0	1	0	1	
	8074	109	2			Lot Code		D	0	30	0	0	1	1	0	0	0	0	Lot 0
	8075	110							0	30	0	0	1	1	0	0	0	0	
	8076	111	1	Current Reference	5V Stressed Environment Reference - 100%=1A	5.0V not used	0	D	60% 69%	10	0	0	0	1	0	0	0	0	for example 0.61A
						20% 29%	1												
						30% 39%	2												
						40% 49%	4												
						50% 59%	8												
						60% 69%	10												
						70% 79%	20												
						80% 89%	40												
						90% 99%	80												
	8077	112	1		3.3V Stressed Environment Reference - 100%=2A	3.3V not used	0	D	30% 39%	02	0	0	0	0	0	0	1	0	for example 0.72A
						20% 29%	1												
						30% 39%	2												
						40% 49%	4												
						50% 59%	8												
						60% 69%	10												
						70% 79%	20												
						80% 89%	40												
						90% 99%	80												
	8078	113	1		APS Stressed Environment Reference - 100%=2A	APS not used	0	D	20% 29%	01	0	0	0	0	0	0	0	1	for example 0.51A
						20% 29%	1												
						30% 39%	2												
						40% 49%	4												
						50% 59%	8												
						60% 69%	10												
						70% 79%	20												
						80% 89%	40												
						90% 99%	80												
	8079	114	1	APS Voltage	Nominal APS Voltage	Unspecified	0	B	1.25	6	0	0	0	0	0	1	1	0	for example 1.25V
						0.9	1												
						1	2												
						1.2	4												
						1.3	8												
						1.5	10												
						1.8	20												
						C	40												
Basic	807A	115	1	DOM Capability	Digital Optical Monitoring Capability	Ext DOM Addr		B		**D1**	1	1	0	1	0	0	0	1	
	807B	116	1	Optional Capability	Low Power Startup Capability Bit Reserved	LPS		A		00	0	0	0	0	0	0	0	0	
						Reserved		A		00	0	0	0	0	0	0	0	0	
	807C	117	1	Reserved				A		00	0	0	0	0	0	0	0	0	
	807D	118	1	Basic Checksum		sum(8007:807C)		D	1361	61	0	1	1	0	0	0	0	1	for example
Customer	807E ~80A	119 ~166	48	Customer Area	Customer Writeable Area			A	all zero	00	0	0	0	0	0	0	0	0	
Vendor	80AE ~8106	167 ~255	89	Vendor Specific	Vendor Specific			A	NA	00	0	0	0	0	0	0	0	0	

Appendix B-3. Alarm and Warning [TRT7063EN]

	hex	DOM Byte #	Size	Name	Description		unit	Value (by unit:dec)	hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	note
Alarm and Warning Threshold	A000	0	2	TMPlimhi	Transceiver Temp High Alarm	LSBit : 1/256	degC	**74**	4A	0	1	0	0	1	0	1	0	note 1,
	A001	1							00	0	0	0	0	0	0	0	0	
	A002	2	2	TMPlimlo	Transceiver Temp Low Alarm	LSBit : 1/256	degC	**-4**	FC	1	1	1	1	1	1	0	0	note 1,
	A003	3							00	0	0	0	0	0	0	0	0	
	A004	4	2	TMPwrnhi	Transceiver Temp High Warning	LSBit : 1/256	degC	70	46	0	1	0	0	0	1	1	0	note 1,
	A005	5							00	0	0	0	0	0	0	0	0	
	A006	6	2	TMPwrnlo	Transceiver Temp Low Warning	LSBit : 1/256	degC	0	00	0	0	0	0	0	0	0	0	note 1,
	A007	7							00	0	0	0	0	0	0	0	0	
	A008	8	2	Vcclimhi	+3.3 V Monitor High Alarm	LSBit : 0.1mV	V	3.63	8D	1	0	0	0	1	1	0	1	note 2
	A009	9							CC	1	1	0	0	1	1	0	0	
	A00A	10	2	Vcclimlo	+3.3 V Monitor Low Alarm	LSBit : 0.1mV	V	2.97	74	0	1	1	1	0	1	0	0	note 2
	A00B	11							04	0	0	0	0	0	1	0	0	
	A00C	12	2	Vccwrnhi	+3.3 V Monitor High Warning	LSBit : 0.1mV	V	3.53	89	1	0	0	0	1	0	0	1	note 2
	A00D	13							E4	1	1	1	0	0	1	0	0	
	A00E	14	2	Vccwrnlo	+3.3 V Monitor Low Warning	LSBit : 0.1mV	V	3.07	77	0	1	1	1	0	1	1	1	note 2
	A00F	15							EC	1	1	1	0	1	1	0	0	
	A010	16	2	MON1limhi	Laser Bias Current High Alarm	**LSBit : 10uA**	mA	BiasMon x 150%	xx	x	x	x	x	x	x	x	x	note 2
	A011	17							xx	x	x	x	x	x	x	x	x	
	A012	18	2	MON1limlo	Laser Bias Current Low Alarm	**LSBit : 10uA**	mA	BiasMon x 50%	xx	x	x	x	x	x	x	x	x	note 2
	A013	19							xx	x	x	x	x	x	x	x	x	
	A014	20	2	MON1wrnhi	Laser Bias Current High Warning	**LSBit : 10uA**	mA	BiasMon x 140%	xx	x	x	x	x	x	x	x	x	note 2
	A015	21							xx	x	x	x	x	x	x	x	x	
	A016	22	2	MON1wrnlo	Laser Bias Current Low Warning	**LSBit : 10uA**	mA	BiasMon x 60%	xx	x	x	x	x	x	x	x	x	note 2
	A017	23							xx	x	x	x	x	x	x	x	x	
	A018	24	2	MON2limhi	Laser Output Power High Alarm	LSBit : 0.1uW	dBm	**8**	**F6**	1	1	1	1	0	1	1	0	note 3
	A019	25							**77**	0	1	1	1	0	1	1	1	
	A01A	26	2	MON2limlo	Laser Output Power Low Alarm	LSBit : 0.1uW	dBm	**-4**	**0F**	0	0	0	0	1	1	1	1	note 3
	A01B	27							**8D**	1	0	0	0	1	1	0	1	
	A01C	28	2	MON2wrnhi	Laser Output Power High Warning	LSBit : 0.1uW	dBm	**4**	**62**	0	1	1	0	0	0	1	0	note 3
	A01D	29							**1E**	0	0	0	1	1	1	1	0	
	A01E	30	2	MON2wrnlo	Laser Output Power Low Warning	LSBit : 0.1uW	dBm	**0**	**27**	0	0	1	0	0	1	1	1	note 3
	A01F	31							**10**	0	0	0	1	0	0	0	0	
	A020	32	2	MON3limhi	Receive Optical Power High Alarm	LSBit : 0.1uW	dBm	**-3**	13	0	0	0	1	0	0	1	1	note 4
	A021	33							93	1	0	0	1	0	0	1	1	
	A022	34	2	MON3limlo	Receive Optical Power Low Alarm	LSBit : 0.1uW	dBm	**-28**	00	0	0	0	0	0	0	0	0	note 4
	A023	35							0F	0	0	0	0	1	1	1	1	
	A024	36	2	MON3wrnhi	Receive Optical Power High Warning	LSBit : 0.1uW	dBm	-7	07	0	0	0	0	0	1	1	1	note 4
	A025	37							CB	1	1	0	0	1	0	1	1	
	A026	38	2	MON3wrnlo	Receive Optical Power Low Warning	LSBit : 0.1uW	dBm	-24	00	0	0	0	0	0	0	0	0	note 4
	A027	39							27	0	0	1	0	0	1	1	1	
	A028 ~A05F	40 ~95	56	Reserved	(for LX4 Xenpak)			all zero	00	0	0	0	0	0	0	0	0	

note 1 : Temperature accuracy is +/-5 degree C over specified operating temperature and voltage
note 2 : Accuracy is +/-10 % of the Opnext set-point over specified operation temperature and voltage.
note 3 : Accuracy is +/-3 dB over average transmit power range,
note 4 : Accuracy is +/-3 dB over average receive power range, from –24 to -7 dBm.