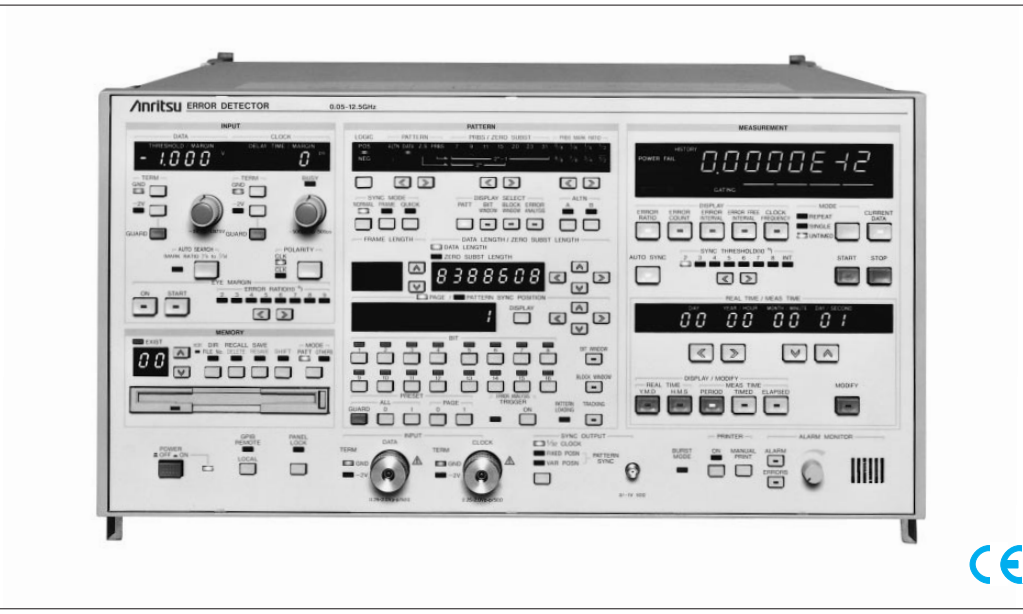
ERROR DETECTOR
MP1764A
12.5 GHz



CE GPIB

The MP1764A is used in combination with the MP1763B Pulse Pattern Generator to detect errors used to evaluate conformity with ITU-T standards. In addition, complicated searching for input thresholds or phase adjustments is simplified with the touch of a single key. These functions are ideally suited for the research and development of ultrahigh-speed logic ICs and digital communication systems.

Features

- Auto-search function for setting optimum values of input threshold and phase setting by a “one-touch” operation
- Synchronization of 8 Mbits pattern is easily made within a short period of time (when in frame mode)
- Errors are detected in intervals as short as 0.1 sec.
- Zero wait time counter gate

Specifications

Operation frequency		0.05 to 12.5 GHz
Data input	Input waveform	NRZ
	Input voltage	0.25 to 2.0 Vp-p
	Threshold voltage variable range	–3.000 to +1.875 Vp-p (1 mV steps)
	Phase margin	≥70 ps (typical value at 10 Gb/s, PRBS 2^{23} – 1, and an input amplitude of 1 Vp-p
	Input sensitivity	50 mVp-p (typical value at 10 Gb/s and PRBS 2^{23} – 1
	Termination	50 Ω connected to GND (other than ECL) or to –2 V (ECL)
	Connector	APC-3.5
Clock input	Input waveform	Rectangular wave (<0.5 GHz), rectangular or sine wave (≥0.5 GHz), duty factor: 50%
	Input voltage	0.25 to 2.0 Vp-p
	Input delay variable range	–500 to +500 ps (1 ps steps)
	Polarity inversion	CLOCK/$\overline{\text{CLOCK}}$ inversion possible
	Termination	50 Ω connected to GND (other than ECL) or –2 V (ECL)
	Connector	APC-3.5
Automatic input data threshold/delay search function		Provided, voltage/delay (vertical/horizontal axis)
Receive pattern	Pseudorandom binary sequence pattern (PRBS)	Pattern: 2^n – 1 (n: 7, 9, 11, 15, 20, 23, 31) Mark ratio: 1/2, 1/4, 1/8, 0/8 (1/2, 3/4, 7/8, 8/8 are possible with logic inversion.) Number of AND bit shift when setting mark ratio: 1, 3 bits (selectable by using DIP switch on rear panel)
	Data pattern*1	Data length: 2 to 8388608 bits, Pattern reset/preset: ALL/PAGE selectable
	Logic inversion	Positive or negative
	Tracking	Information of pattern set by the error detector is sent to the pulse pattern generator via GPIB.
	Alternate pattern	A/B pattern word length: 128 to 4194304 bits (128 bits steps), Number of loops: Controlled using external signal
	Zero substitution pattern	Zero bit length: 1 to (pattern length –1) bits, Pattern length: 2^n (n: 7, 9, 11, 15)

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Sync mode	Normal	Valid for PRBS and programmable pattern
	Frame	Valid for programmable pattern (≥128 bits)
	Frame bit length	4 to 32 bits (4-bit step)
	Quick	Valid for DATA, zero subset pattern
Error detection mode		Omission insertion, total (selectable with DIP switch on rear panel)
Synchronous threshold		Preset value or 10^{-n} (n: 2, 3, 4, 5, 6, 7, 8)
Measure-ment item	Error rate	0.0000 x 10^{-16} to 1.0000 x 10^{-0}
	Number of errors	0 to 9.9999 x 10^{16}
	Error interval (asynchronous)	0 to 9999999 (interval: 1 ms, 10 ms, 100 ms, 1 s)
	Error free interval (EFI)	0.0000% to 100.0000% (interval: 1 ms, 10 ms, 100 ms, 1 s)
	Clock frequency	0.05 to 12.5 GHz, Resolution: 1 kHz, Error: ± (10 ppm + 1 kHz)
Eye margin measurement function		Provided
Error performance data calculation function		Provided [results are output to external printer or external instruments via GPIB.]
Measurement CH mask		1 to 32 ch (settable independently)
Block windowError for any block of 32-bit segments can be measured.		
Error analysis (option 01)		Pattern (256 bits in total) before and after bit in which error occurred is stored.
Current data	Display cycle	0.1, 0.2 s (selectable with rear panel DIP switch)
	Display mode	INTERVAL/CYCLE (selectable with rear panel DIP switch)
Measurement mode		Repeat, single, untimed
Measurement time		1 s to 99 days 23 hours 59 minutes 59 seconds (1 second steps)
Timer		Year, month, day, hour, minute, second
Auxiliary output	Sync signal output	Number of outputs CLOCK: 1 (1/32 clock, fixed position pattern or variable position pattern selectable) Level: 0/–1 V; Connector: SMA
	ORED ERROR output (DIRECT)	Number of outputs: 1(1/32 ored error); Level: 0/–1 V; Connector: SMA
	ORED ERROR output (STRETCHED)	Output level: TTL; Pulse width: 350 ns (typical); Connector: BNC
	Alarm output	Output condition: Power recovery, clock loss, asynchronous Output level: TTL Connector: BNC
	Frame sync output	Level: 0/–1 V; Connector: SMA
	Sync gain output	Output level: 0/–1 V; Connector: SMA
Auxiliary input	External mask input	Input level: 0/–1 V; Connector: SMA
	Resync input	Input level: 0/–1 V; Connector: SMA
	Alternate A/B switching input	Input level: ECL; Connector: SMA
Display	Measurement results	7 segments, 7 digits
	Gate time	12-segment bar graph
	Alarm	Error occurrence: Red lamp comes on; Clock loss: Orange lamp comes on; Sync loss: Orange lamp comes on
Audible alarm		Provided (error sound)
External control		GPIB (IEEE 488.2)
Operating temperature range		0˚ to +50˚C (however, 5˚ to 45˚C for parameter memory floppy disk)
Parameter memory		Media: 3.5 inch floppy disk (2HD, 2DD) Format: MS-DOS (Rev. 3.1)*2 Content: Programmable pattern and other parameters
Power		*3Vac ±10%, 50/60 Hz (100/200 V selectable), ≤800 VA
Dimensions and mass		426 (W) x 221.5 (H) x 451 (D) mm, ≤35 kg
EMC		EN55011: 1991, Group 1, Class A EN50082-1: 1992 Harmonic current emissions: EN61000-3-2 (1995)
Safety		EN61010-1: 1993 (Installation Category II, Pollution Degree II)

*1: Relationship between number of pages and items of word length, number of words, and data length

• Numerical relation between data length and step width

Data length	Step width
2 to 65536	1 step
65536 to 131072	2 step
131072 to 262144	4 step
262144 to 524288	8 step
524228 to 1048576	16 step
1048576 to 2097152	32 step
2097152 to 4194304	64 step
4194304 to 8388608	128 step

• Relationship between pages of WORD mode and DATA mode

Output pattern/mode	Variable page range
DATA	1 to < data length/16, 1 step width (up to quotient value when the remainder is 0, up to quotient value +1, 1 step width) Data length — Number of pages 2 to 16 — 1 17 to 32 — 2 33 to 48 — 3 ≥49 — ≥4

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*2: MS-DOS is a registered trade mark of Microsoft Corporation.

• Floppy disk format

Media type	Memory capacity	Sector length	Sector number	Track number	Recording surface
2HD	1440 KB	512 bytes	18	80	Double-sided
2DD	720 KB	512 bytes	9	80	Double-sided
2HD	1232 KB	1024 bytes	8	77	Double-sided
2DD	640 KB	512 bytes	8	80	Double-sided

*3: Specify one nominal line voltage between 100 and 240 V when ordering. Maximum operating voltage is 250 V.

Ordering information

Please specify model/order number, name, and quantity when ordering.

Model/Order No.	Name	
	Main frame	
MP1764A	Error Detector	
	Standard accessories	
J0500A	Semi-rigid cable (SMA-P • SX-36 • SMA-P), 0.5 m:	2 pcs
J0515	Coaxial cable (SMA-P • RG-58A/U • SMA-P), 1 m:	2 pcs
J0496	APC-3.5 J-J connector:	2 pcs
J0008	GPIB cable, 2 m:	1 pc
J0491	Power cord:	1 pc
Z0168	3.5 inch floppy disk (MF2HD-3.5MF):	2 pcs
F0079	Fuse, 10 A (for 100 V mains):	2 pcs
F0014	Fuse, 6.3 A (for 200 V mains):	2 pcs
W0887AE	MP1764A operation manual:	1 copy
W0888AE	MP1764A GPIB operation manual:	1 copy
	Option	
MP1764A-01	Error analysis	
	Optional accessories	
J0500B	Semi-rigid cable (SMA-P • SX-36 • SMA-P), 1 m	
J0322A	Coaxial cable (11SMA •SUCOFLEX104 •11SMA), 0.5 m	
J0322B	Coaxial cable (11SMA • SUCOFLEX104 • 11SMA), 1 m	
J0498	Coaxial cable (APC3.5-P • – • APC3.5-P), 0.5 m (double shielded)	
J0499	Coaxial cable (APC3.5-P • – • APC3.5-P), 1 m (double shielded)	
J0007	GPIB cable, 1 m	
Z0054	3.5 inch floppy disk (MF2DD-3.5MF)	
MB24B	Portable Test Rack (rating current of power cord and plug: 20A)	
B0413A	Carrying case	
B0163	Soft carrying case	
B0044	Rack mount (for 1MW • 5U panel)	
W0887BE	MP1764A service manual	